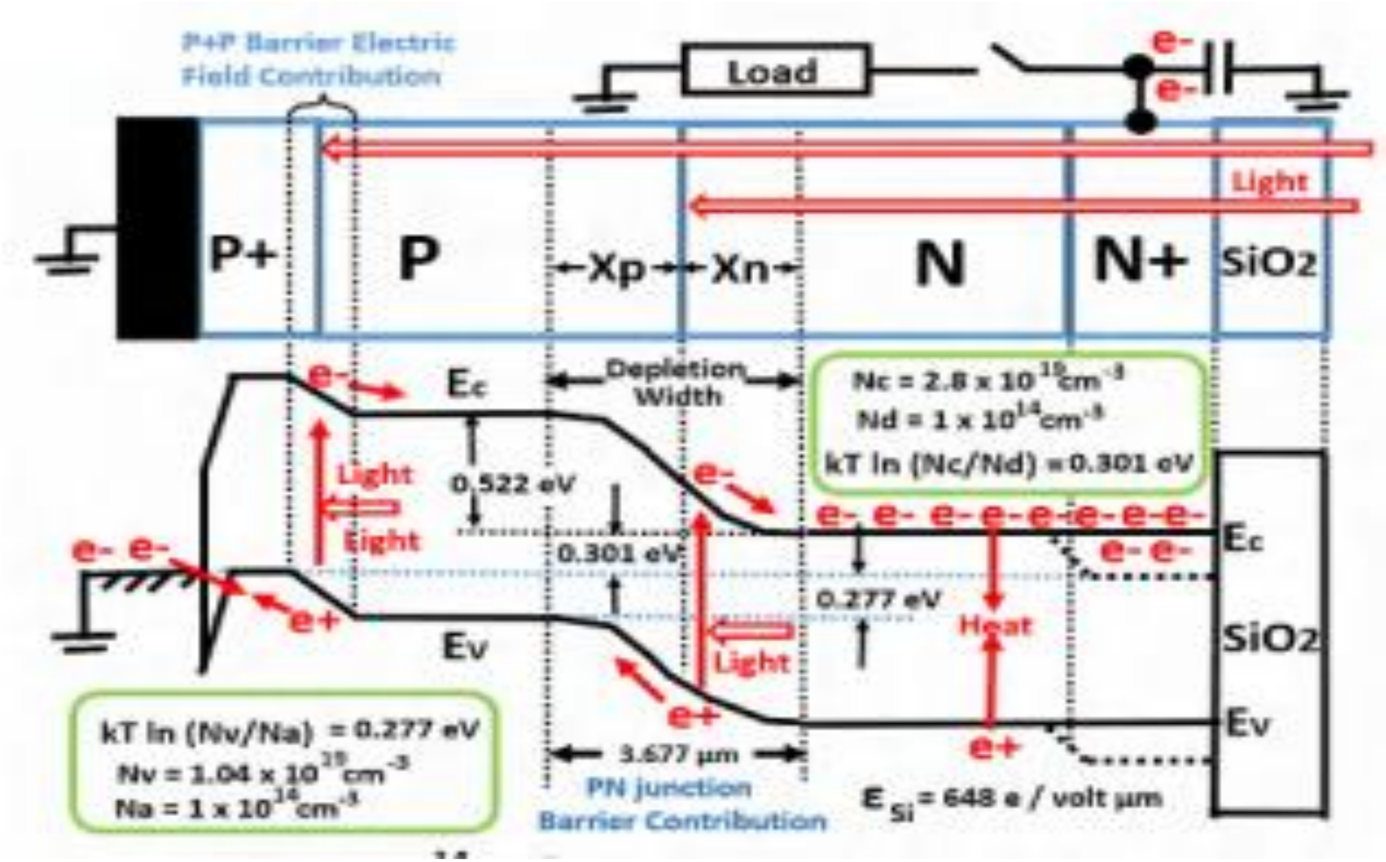
# 8 Double Junction Photo Transistor type Solar Cell

## Under Construction

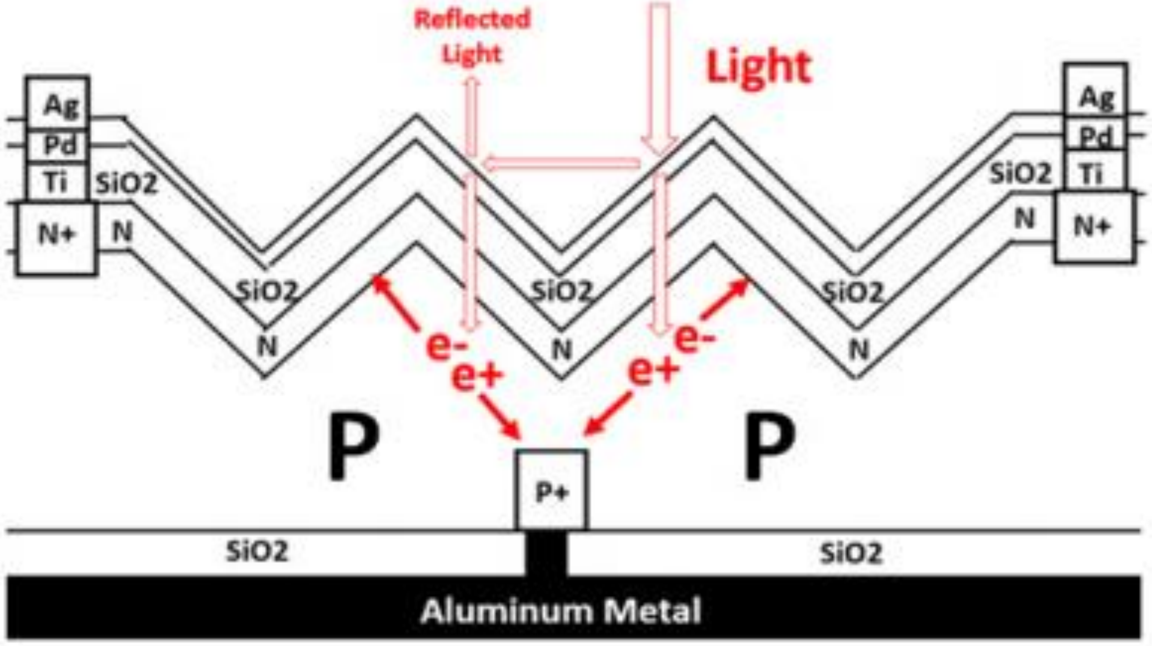
# 8 Double Junction Photo Transistor type Solar Cell

A typical conventional solar cell is very similar to the N+P junction photodiode used in classical MOS image sensors with poor quantum efficiency.



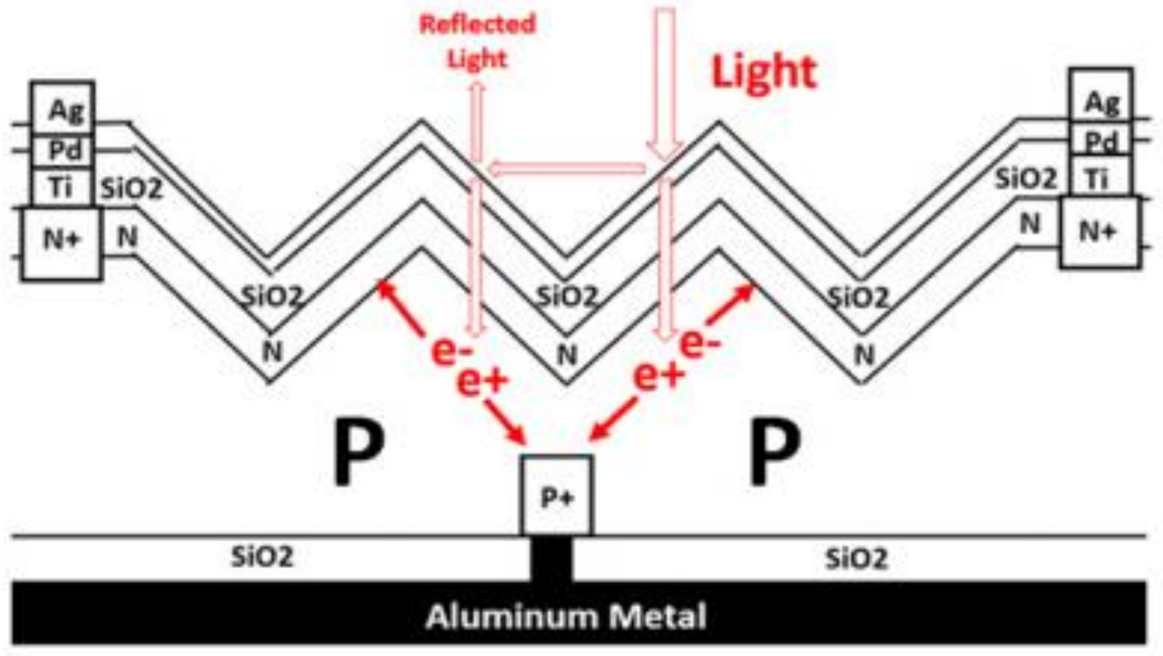
# 8 Double Junction Photo Transistor type Solar Cell

A typical solar panel on the market today has a large area semiconductor device structure of a single junction floating photodiode. Although fabricated by an economically simple semiconductor process technology, cares are taken to prevent the surface reflection loss.



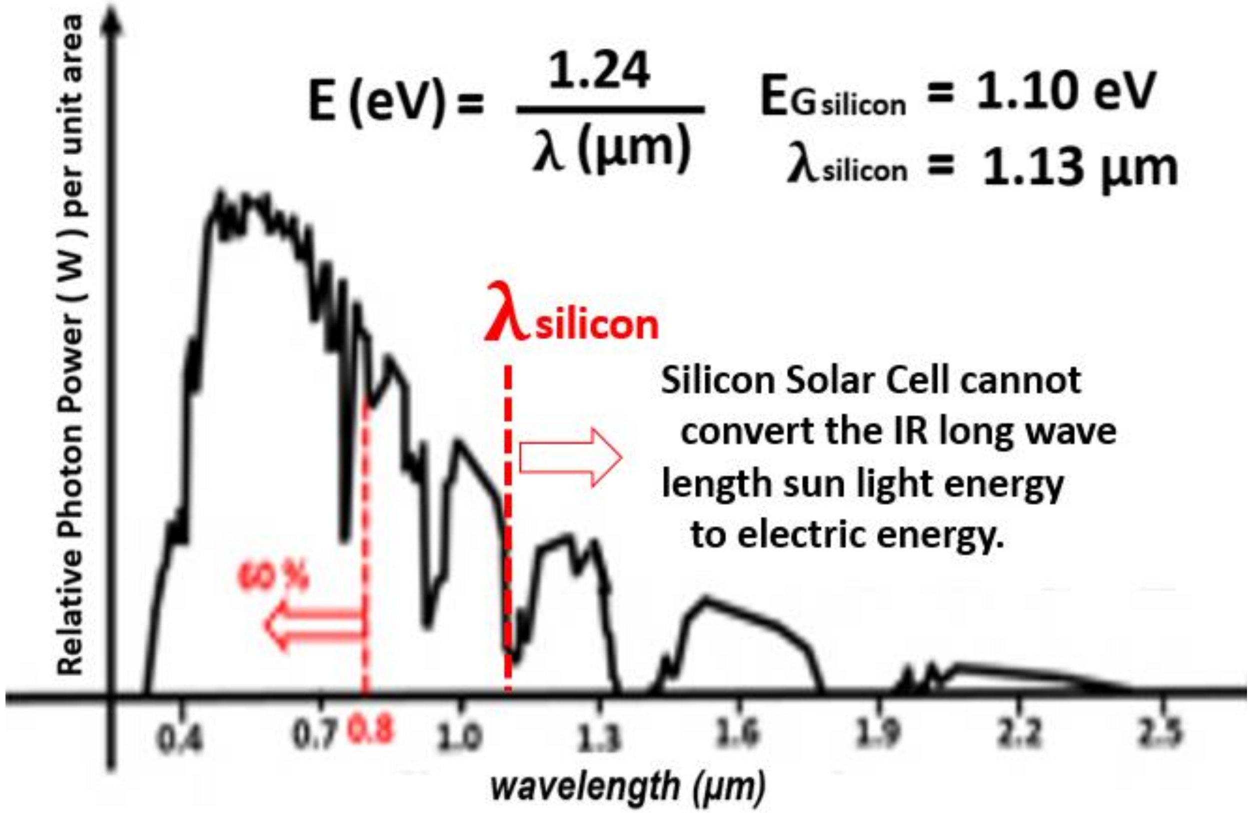
# 8 Double Junction Photo Transistor type Solar Cell

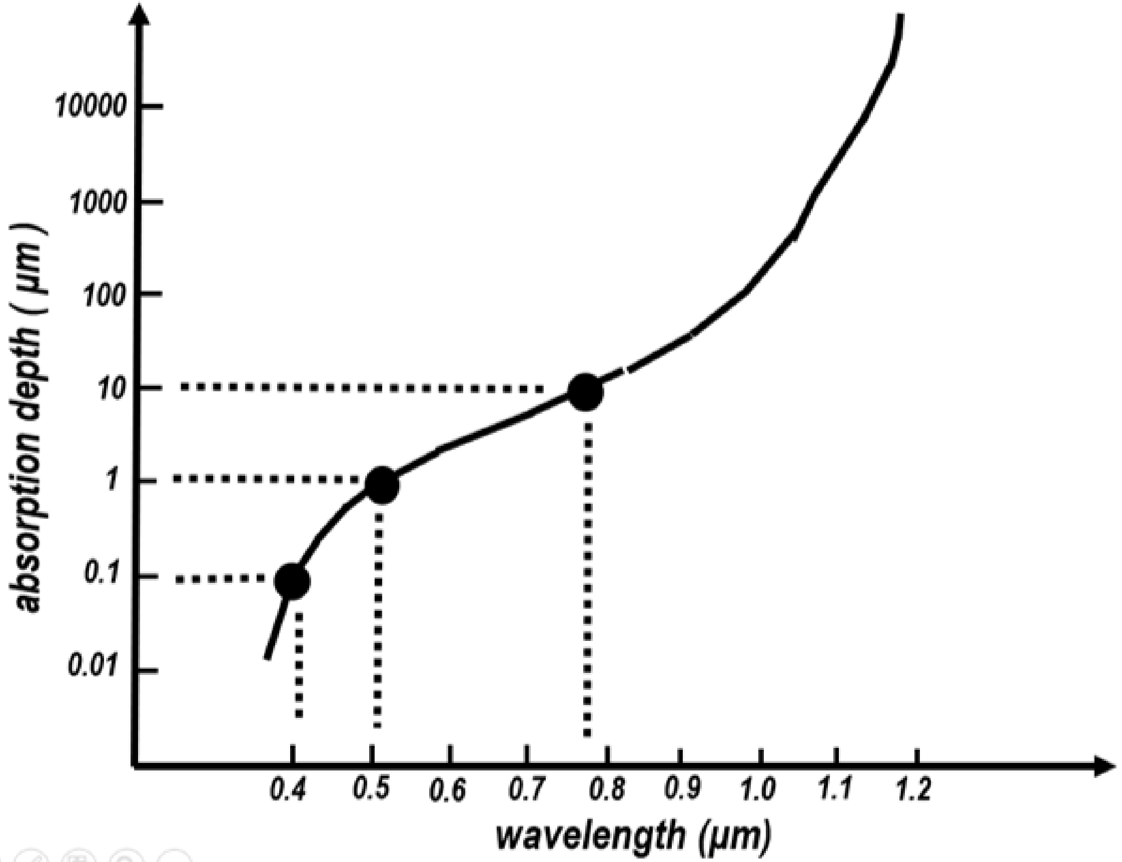
The physical principle under lining the photon to electron energy conversion process is identical both in a solar cell and an image sensor. Silicon wafers are attractive cost-wise and used widely.



# 8 Double Junction Photo Transistor type Solar Cell

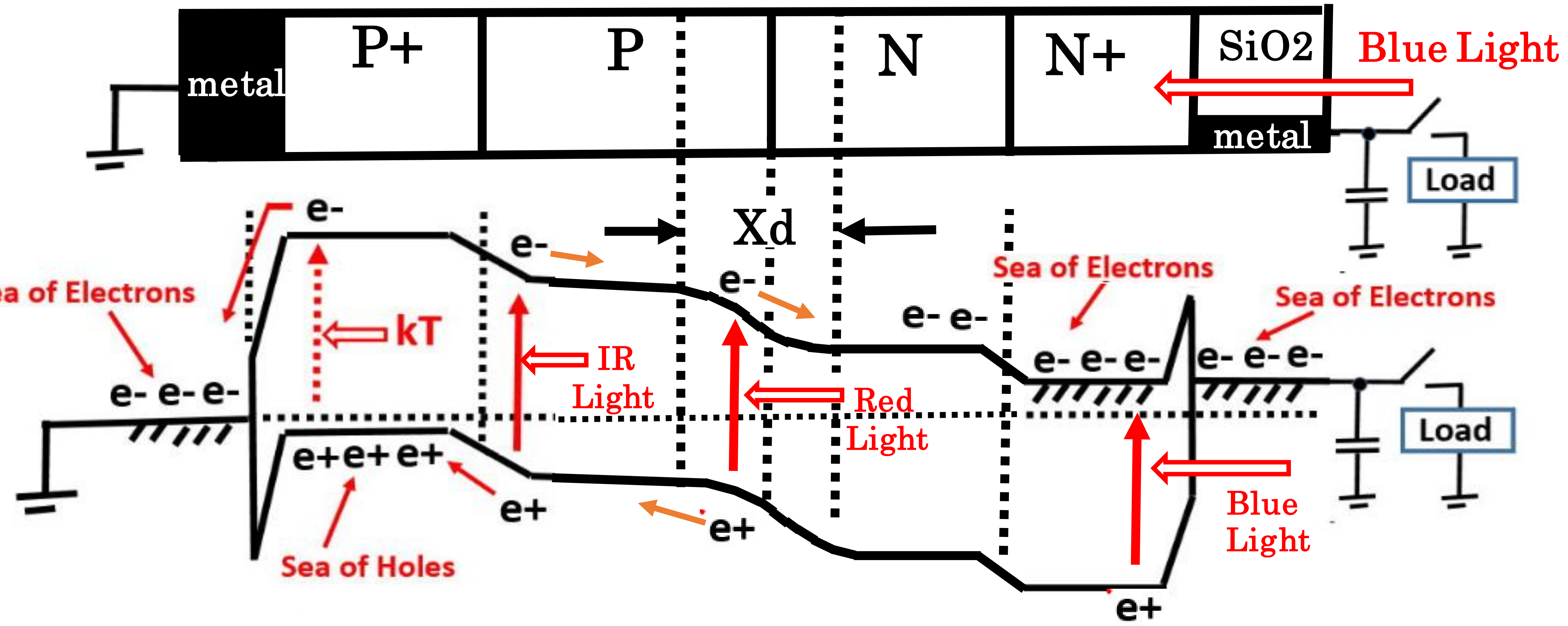
The sun light contains a large portion of the short wave energy spectrum. However the short wave blue light cannot penetrate the silicon wafer more than 0.2 μm in depth.



## 8 Double Junction Photo Transistor type Solar Cell

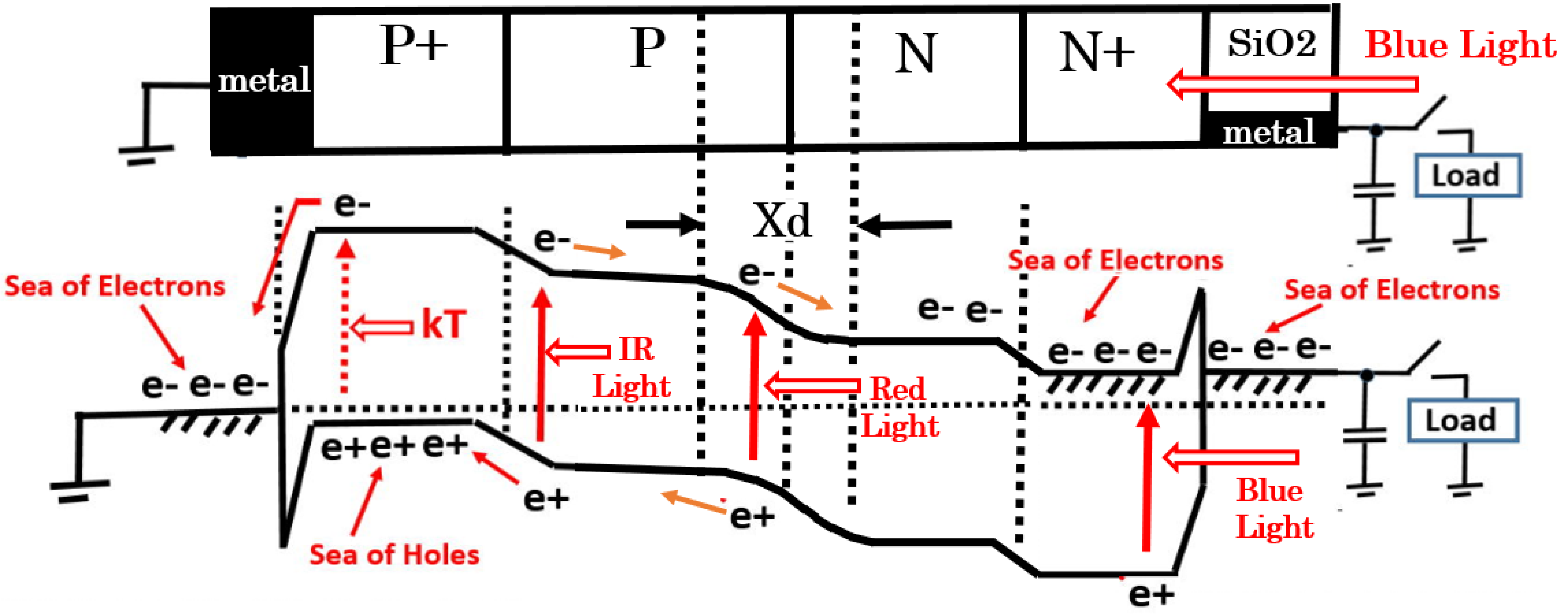
However the conventional simple N+P junction type photodiode has the floating N+ type charge collecting surface layer of the majority carrier electron accumulation.



# 8 Double Junction Photo Transistor type Solar Cell

The silicon surface has a flat potential and no electric filed to separate the photo electron and hole pairs generated by the sun light.

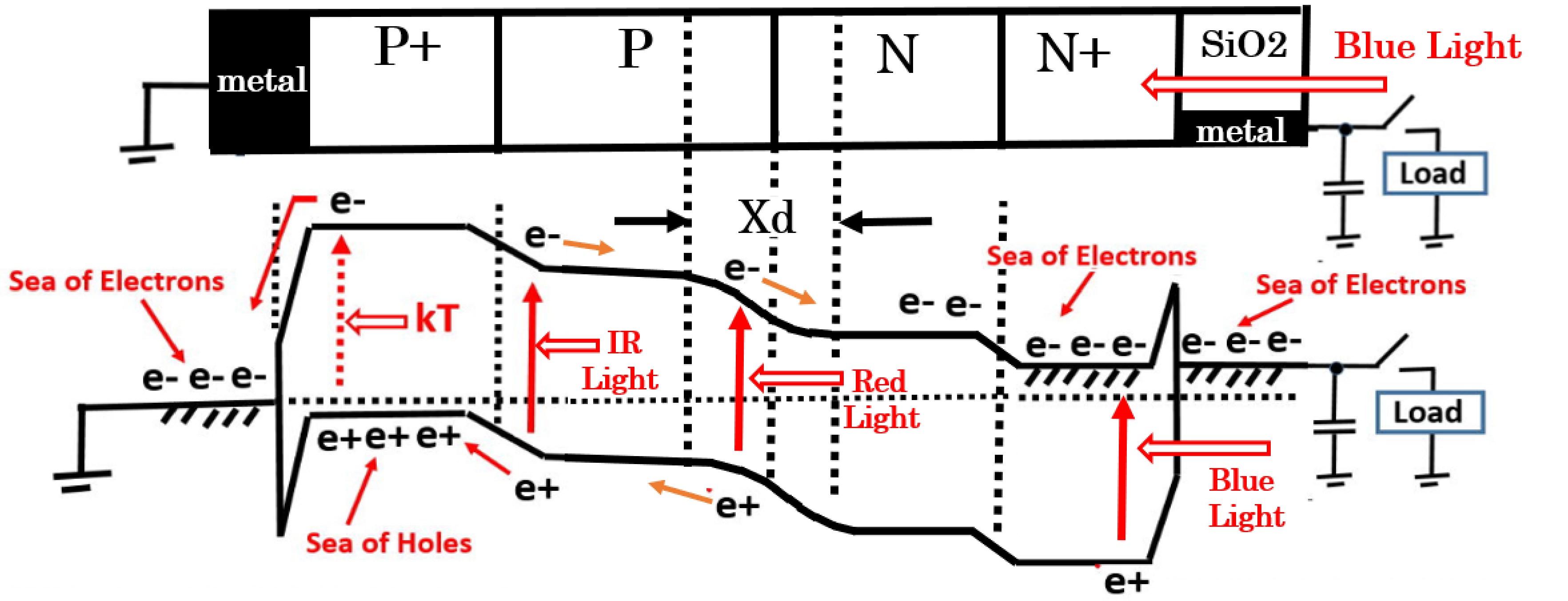
Since the short wave blue light incident to the surface cannot penetrate more than 0.2 μm depth in silicon, the electron and hole pairs generated by photons feel no electric field to separate each other.



# 8 Double Junction Photo Transistor type Solar Cell

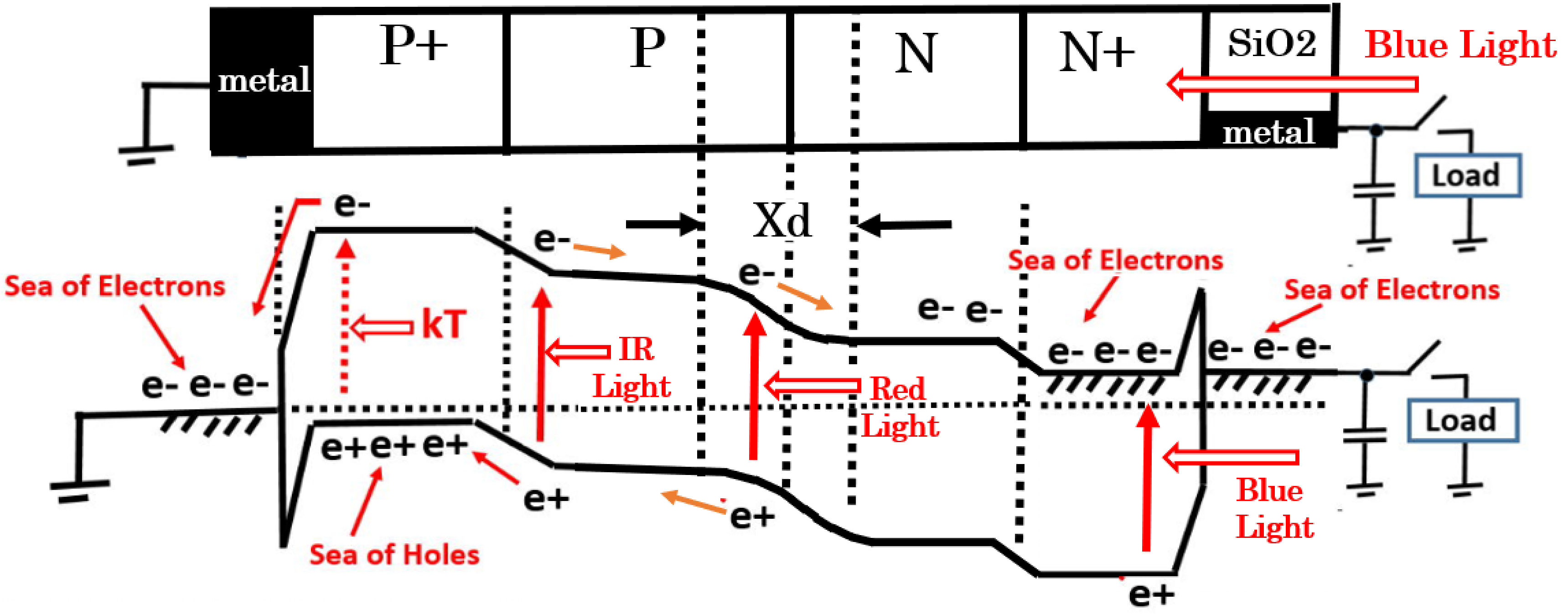
The electron and hole pairs generated by photons will stay where they were and eventually they will meet each other again and recombine to become heat.

In this way, the short wave blue energy spectrum of the sun light does not contribute the solar cell photon to electron energy conversion efficiency.



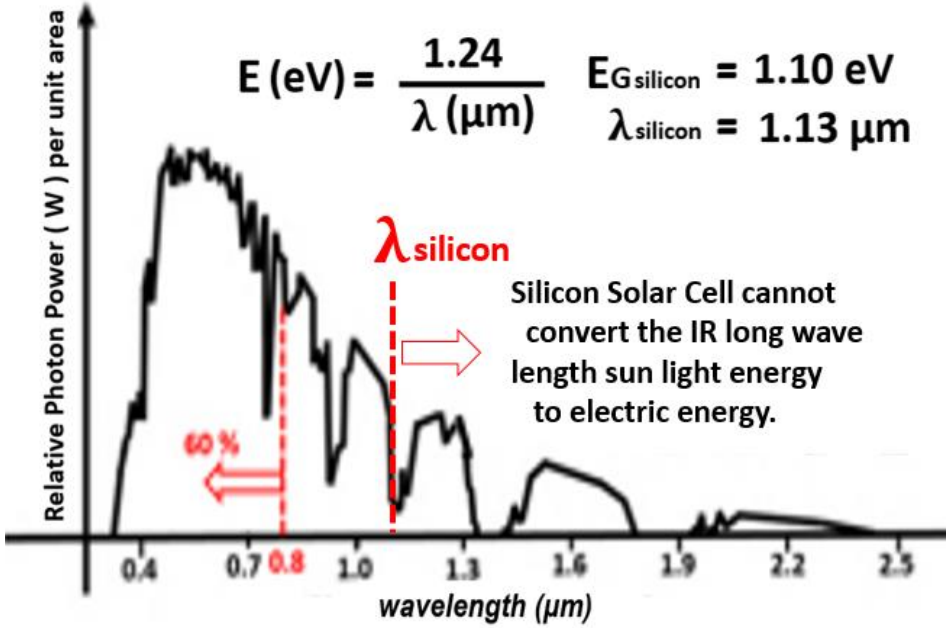
# 8 Double Junction Photo Transistor type Solar Cell

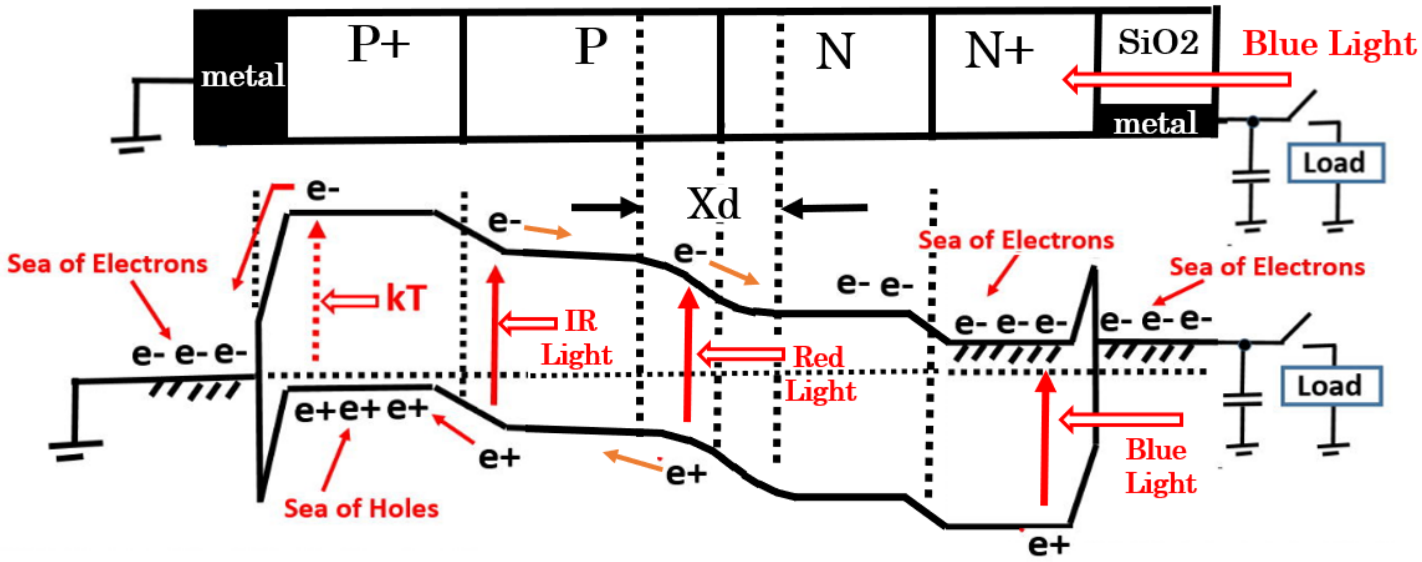
Only the long wave length light low energy photons can be converted into electron energy in the depletion region of the very narrow width Xd . With the same reason, the classical simple N+P single floating junction photodiode used in the MOS type CTD image sensors had a poor short blue light sensitivity. So is the conventional N+P junction type solar cell of low efficiency.



# 8 Double Junction Photo Transistor type Solar Cell

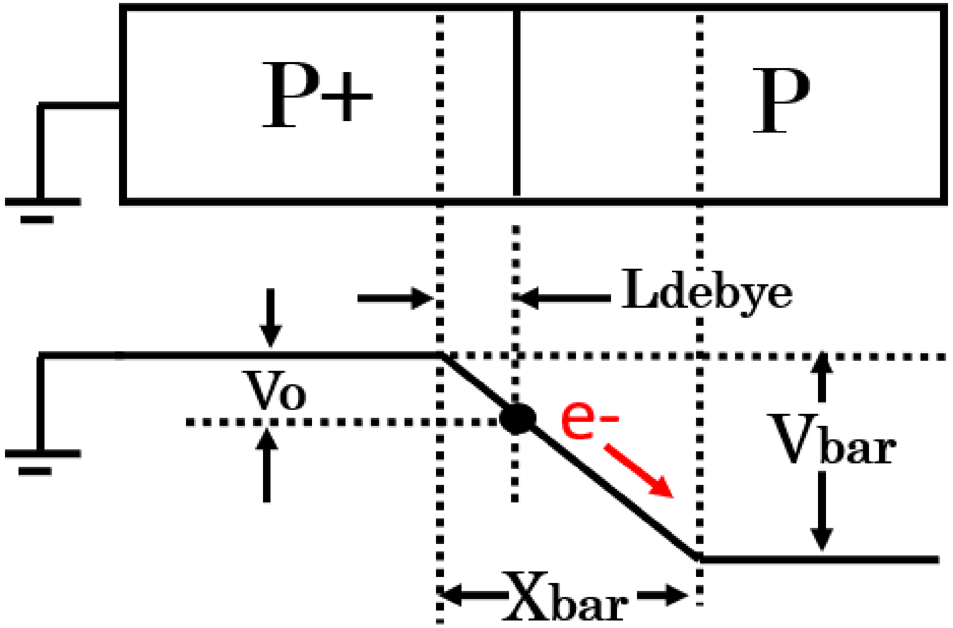
The IR light can reach the back P+P heavily doped region and if the photon energy is larger than the silicon energy gap $E_G = 1.10$ eV, the electron and hole pairs can be generated and will contribute the solar cell photon energy conversion efficiency. This observation means that, if the heavily doped P+P profile is formed in the silicon surface of the light illumination side, the short wave light also contributes the solar cell photon energy conversion efficiency.



# 8 Double Junction Photo Transistor type Solar Cell

The barrier potential $V_{bar}$ is given as $V_{bar} = kT \ln ( NA+ / NA )$ and the barrier electric field region has the width $X_{bar}$ which can be estimated roughly as $X_{bar} = \{ 1 + \ln ( N_A+ / N_A ) \} L_{debye}$ where the Debye length $L_{debye}$ is given by $L_{debye} = \sqrt{\varepsilon_{Si}\, kT / N_A+} =$ 0.0407 μm for $N_A+ = 10000$ e $\mu m^{-3}$, we then have $X_{bar} = 7.91\, L_{debye} = 0.322$ μm for the low density P substrate of $N_A = 100$ e $\mu m^{-3}$. Here we use $\varepsilon_{Si} = 648$ e / volt・μm and $kT = 0.0256$ volt for our convenience.




$$V_{bar} = kT \ln \left( \frac{NA+}{NA} \right)$$

$$X_{bar} = \left\{ 1 + \ln \left( \frac{NA+}{NA} \right) \right\} L_{debye}$$

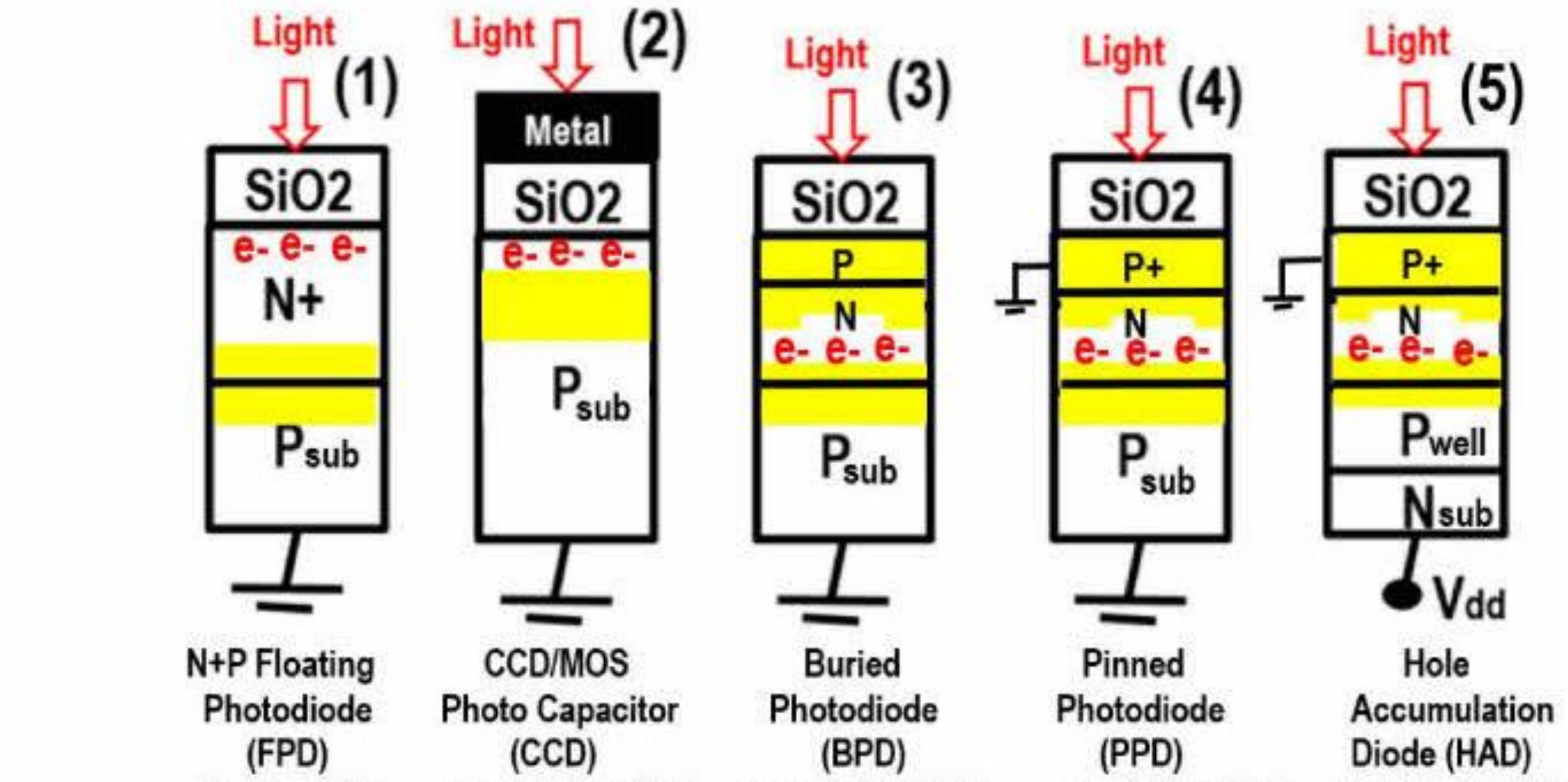
$$L_{debye} = \sqrt{\frac{\varepsilon_{Si} kT}{N_A+}}$$

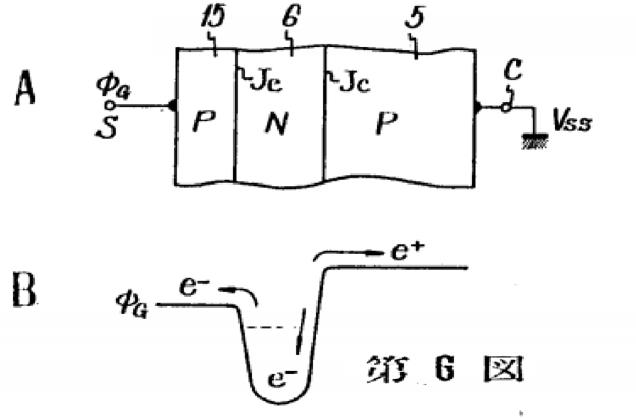
$$\frac{V_o}{kT} = 1 - \frac{\ln \left( \frac{NA+}{NA} \right)}{\left( \frac{NA+}{NA} \right) - 1}$$

# 8 Double Junction Photo Transistor type Solar Cell

Instead in 1975, Hagiwara at Sony proposed a double junction P+NP type dynamic photo transistor with more useful extra function capability.

Different kinds of Photon Detecting Device (PDD)



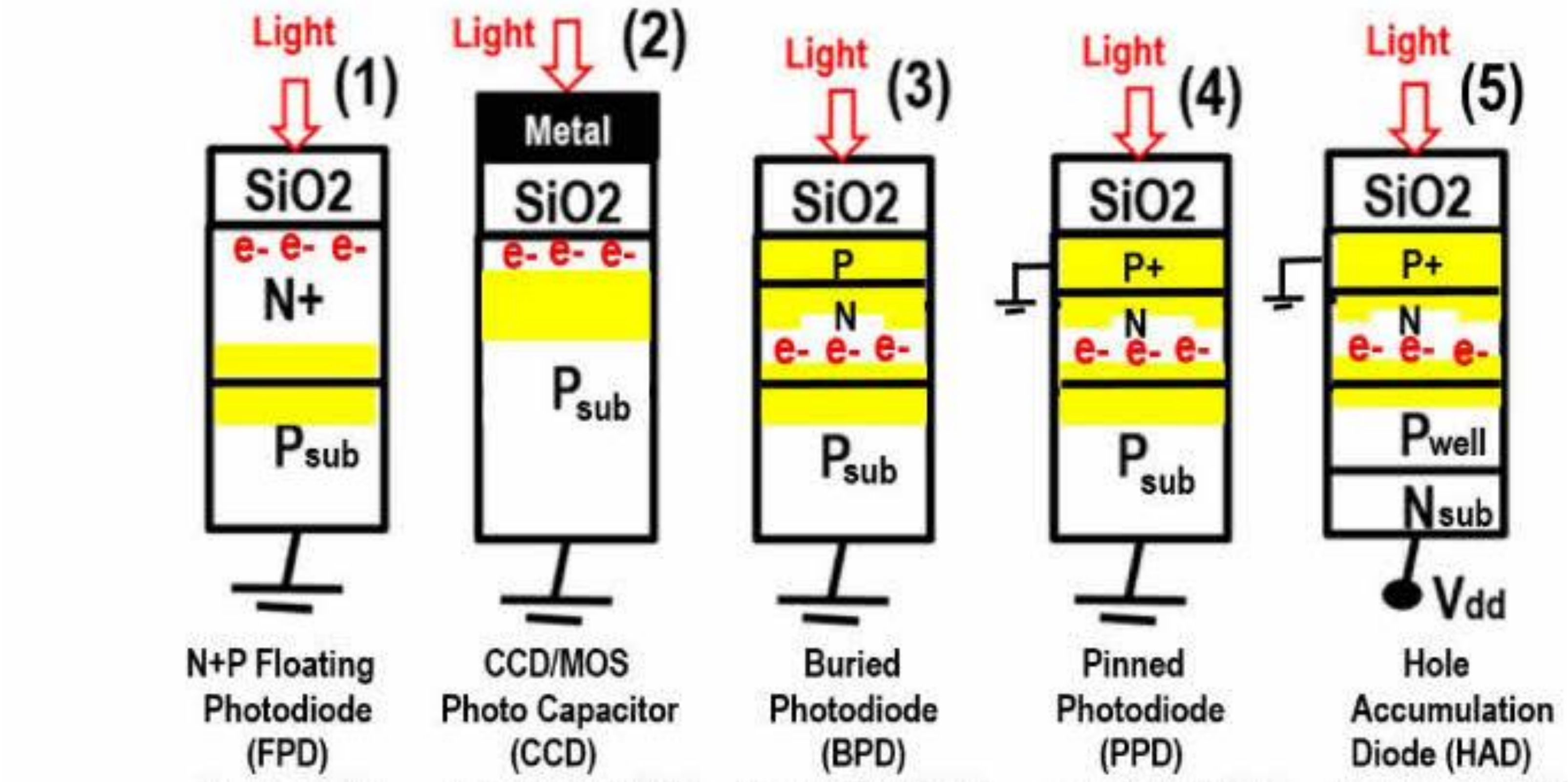

The dynamic photo transistor shown in Fig. 6 of JPA 1975-134985

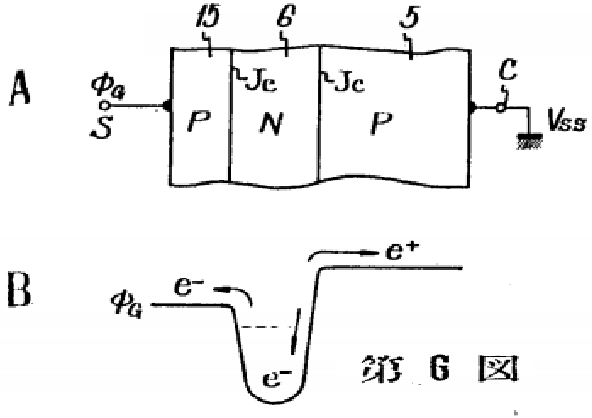
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

# 8 Double Junction Photo Transistor type Solar Cell

**The cost is the issue. However many diligent research and development efforts have been performed to improve the solar cell energy conversion efficiency.**

Different kinds of Photon Detecting Device (PDD)

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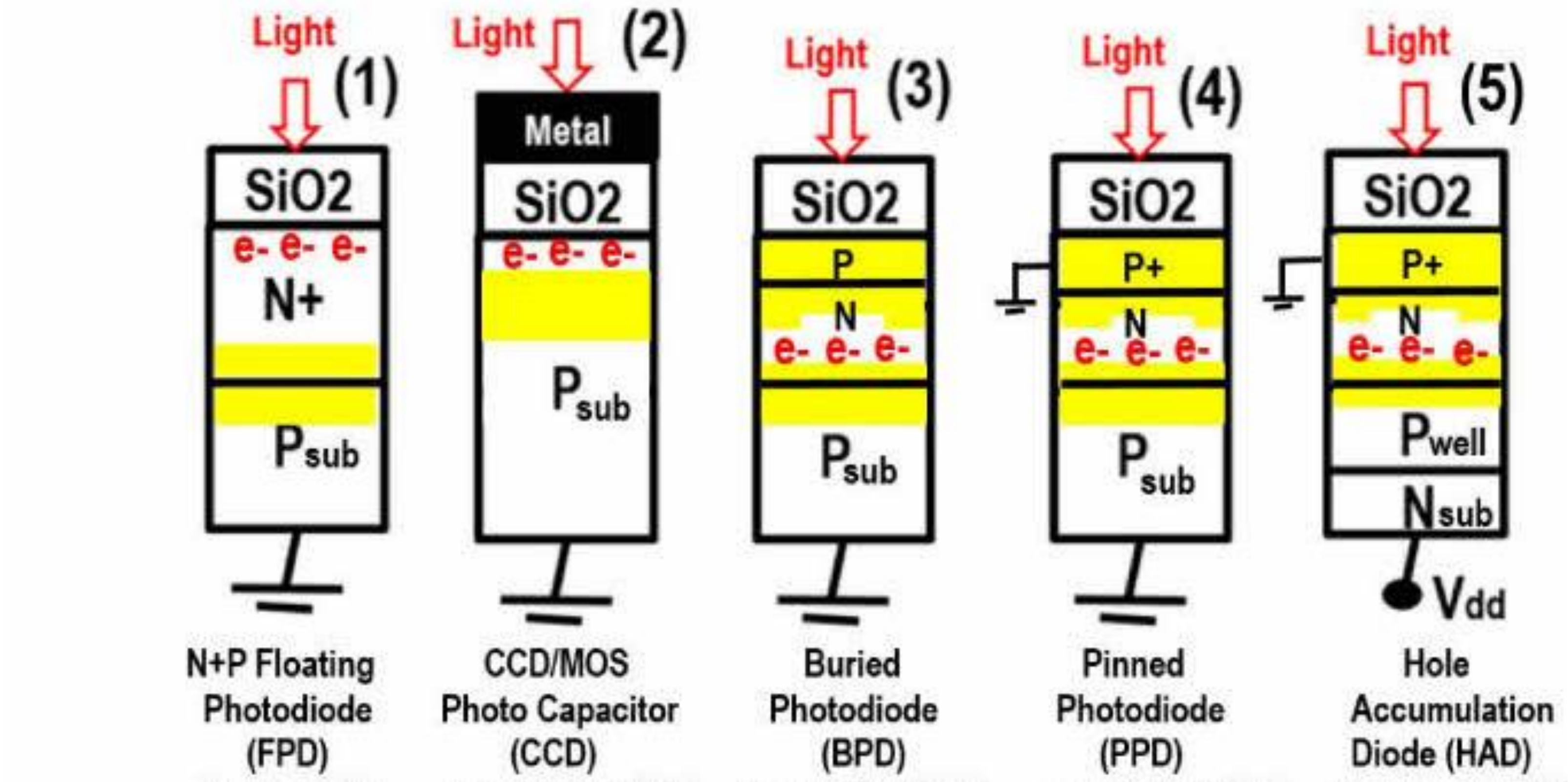
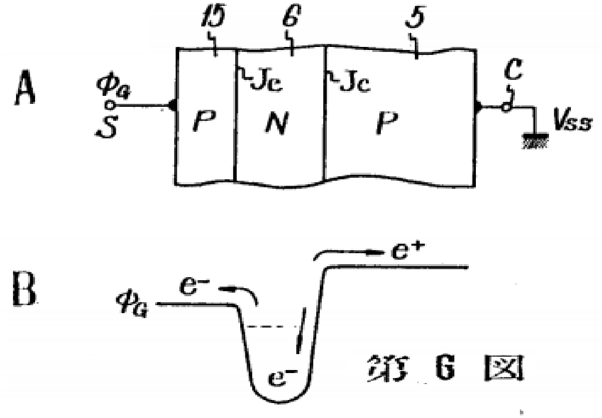
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

# 8 Double Junction Photo Transistor type Solar Cell

The double junction P+NP type dynamic photo transistor has been intensively studied and well understood now, being powered by the image sensor market.

Different kinds of Photon Detecting Device (PDD)



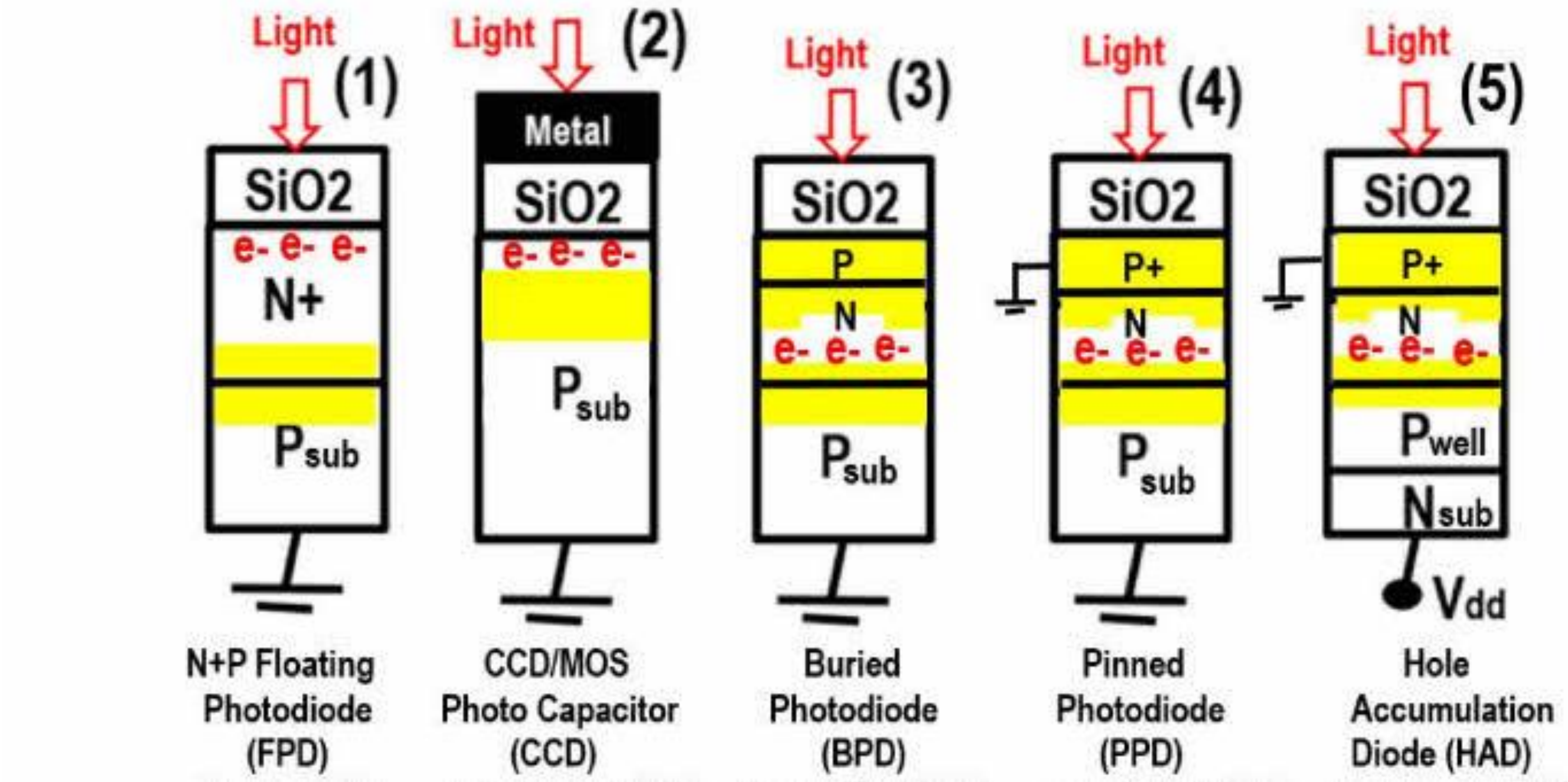

The dynamic photo transistor shown in Fig. 6 of JPA 1975-134985

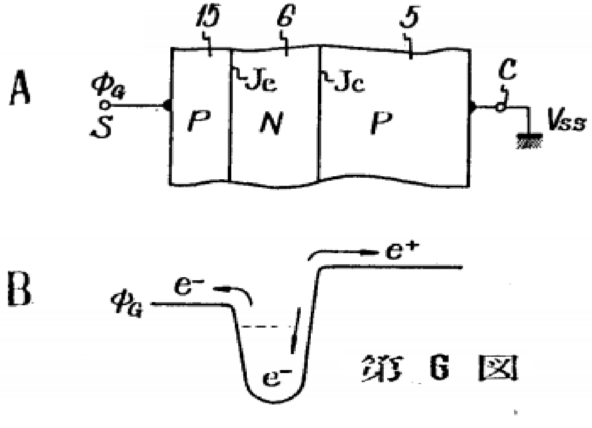
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

# 8 Double Junction Photo Transistor type Solar Cell

The most important feature of the double junction P+NP type dynamic photo transistor is the complete charge transfer without a single photo electron loss.

Different kinds of Photon Detecting Device (PDD)



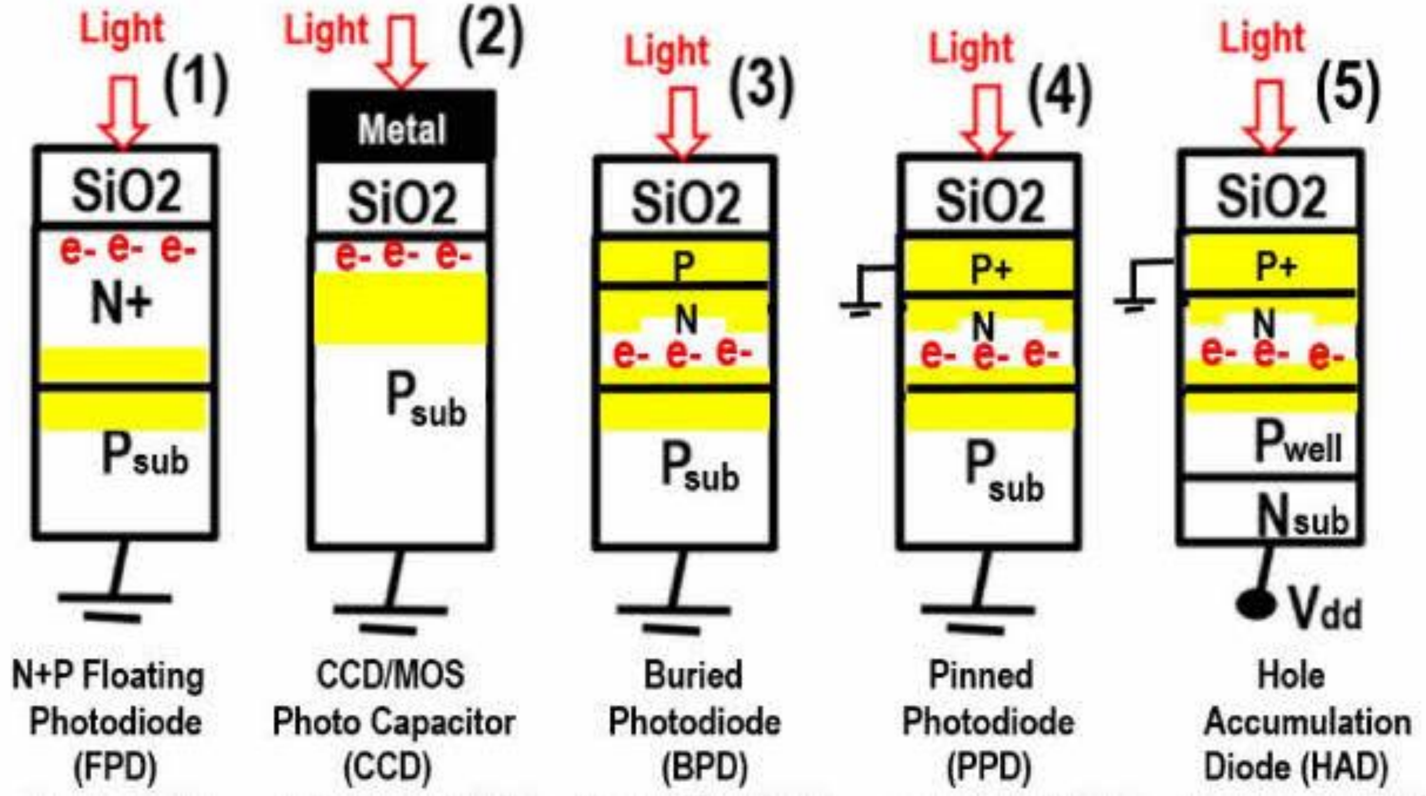

The dynamic photo transistor shown in Fig. 6 of JPA 1975-134985

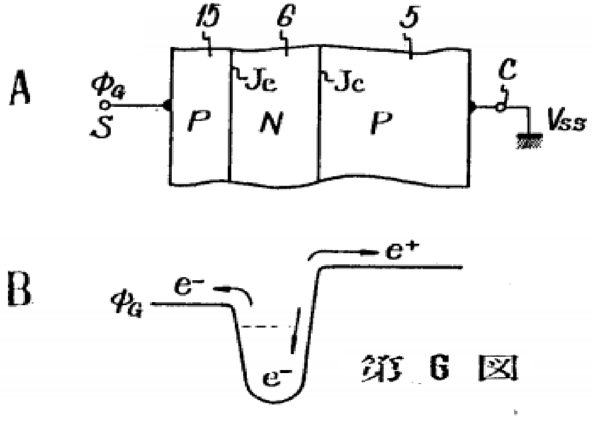
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

# 8 Double Junction Photo Transistor type Solar Cell

On the other hand, as explained before, the conventional single junction type floating photodiode used in the present solar cells lose many photo electrons.

Different kinds of Photon Detecting Device (PDD)



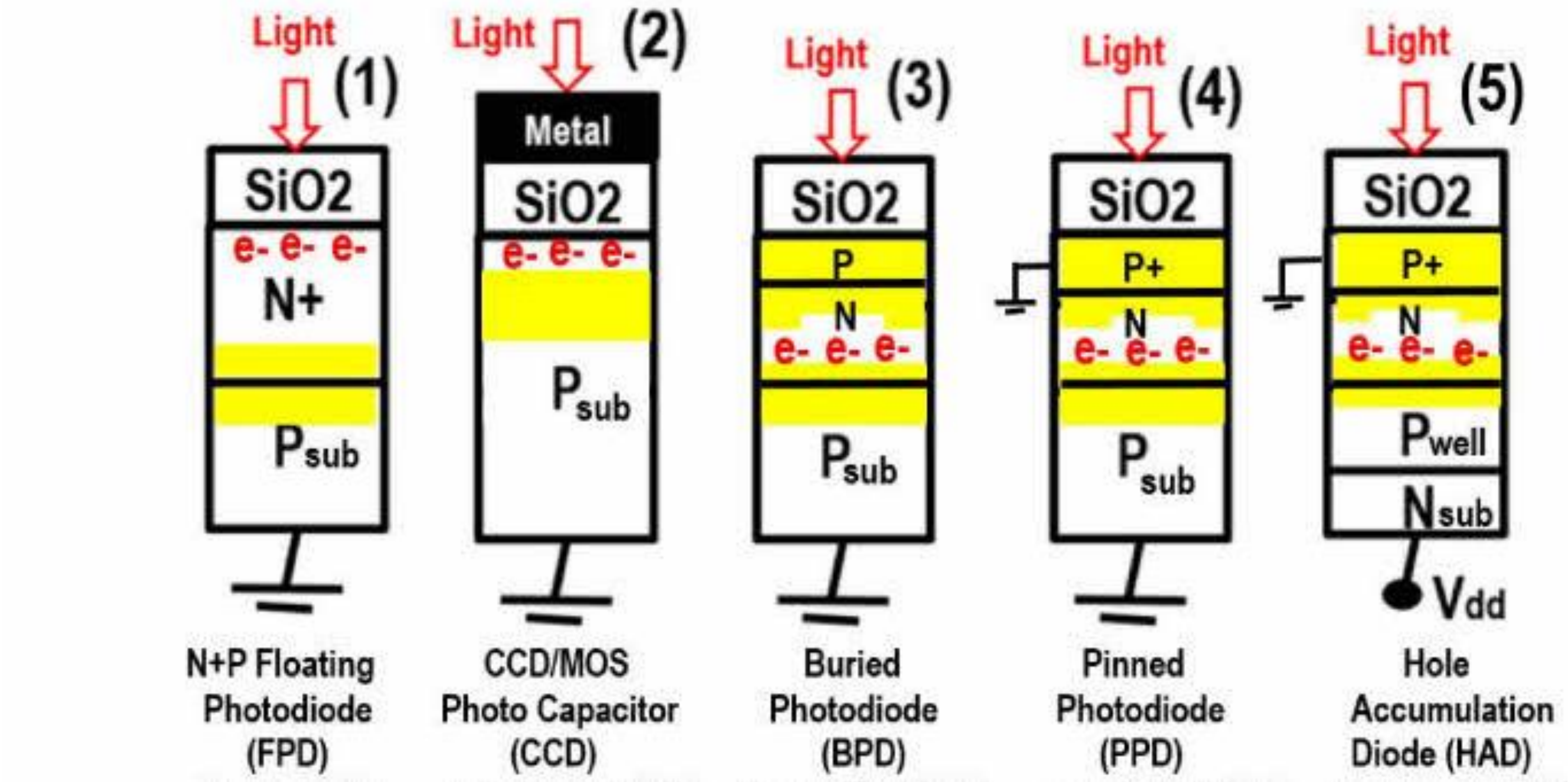

The dynamic photo transistor shown in Fig. 6 of JPA 1975-134985

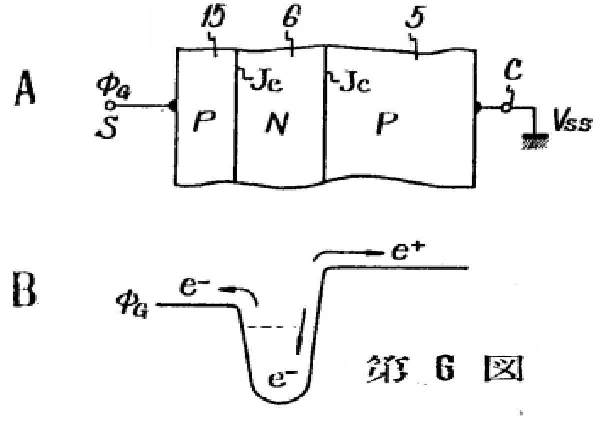
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

# 8 Double Junction Photo Transistor type Solar Cell

If the double junction type dynamic photo transistor is used for the solar cell in a proper process and device design, a single photo electron may not be lost.

Different kinds of Photon Detecting Device (PDD)

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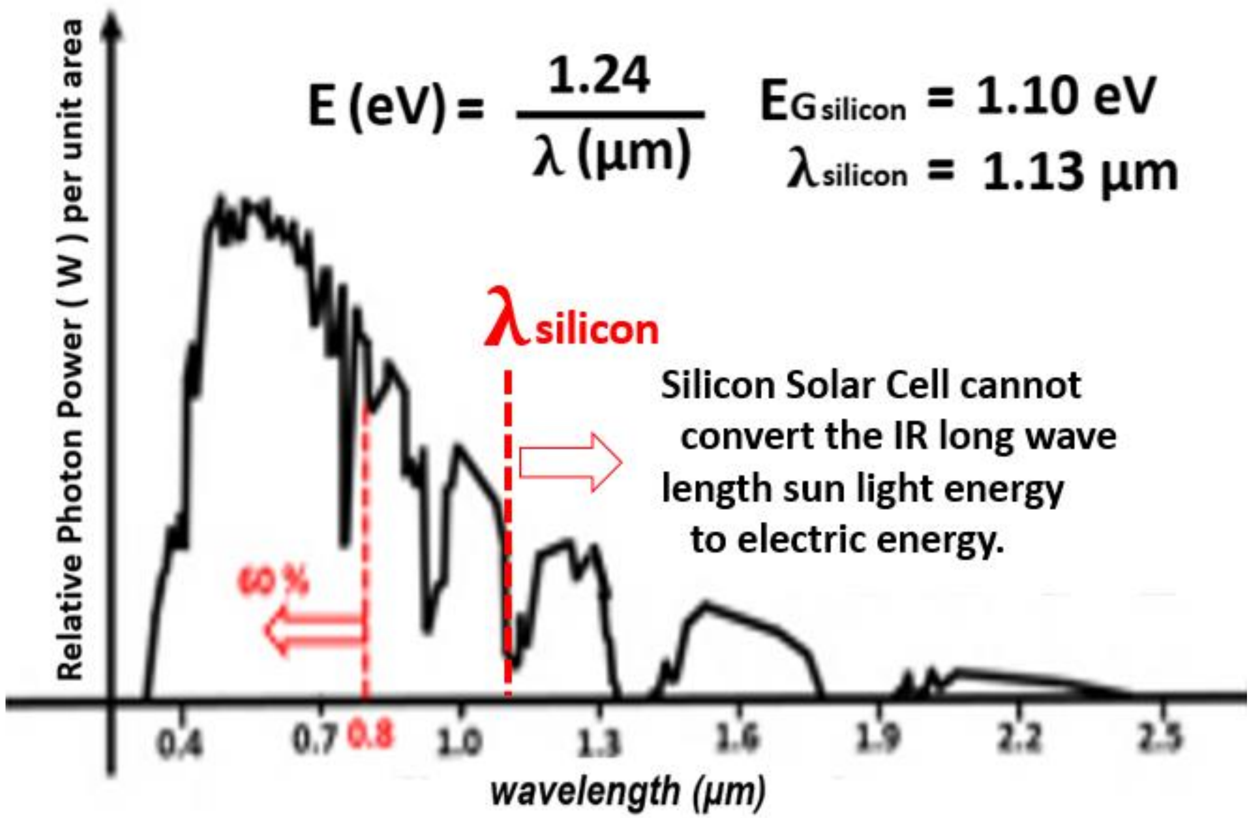
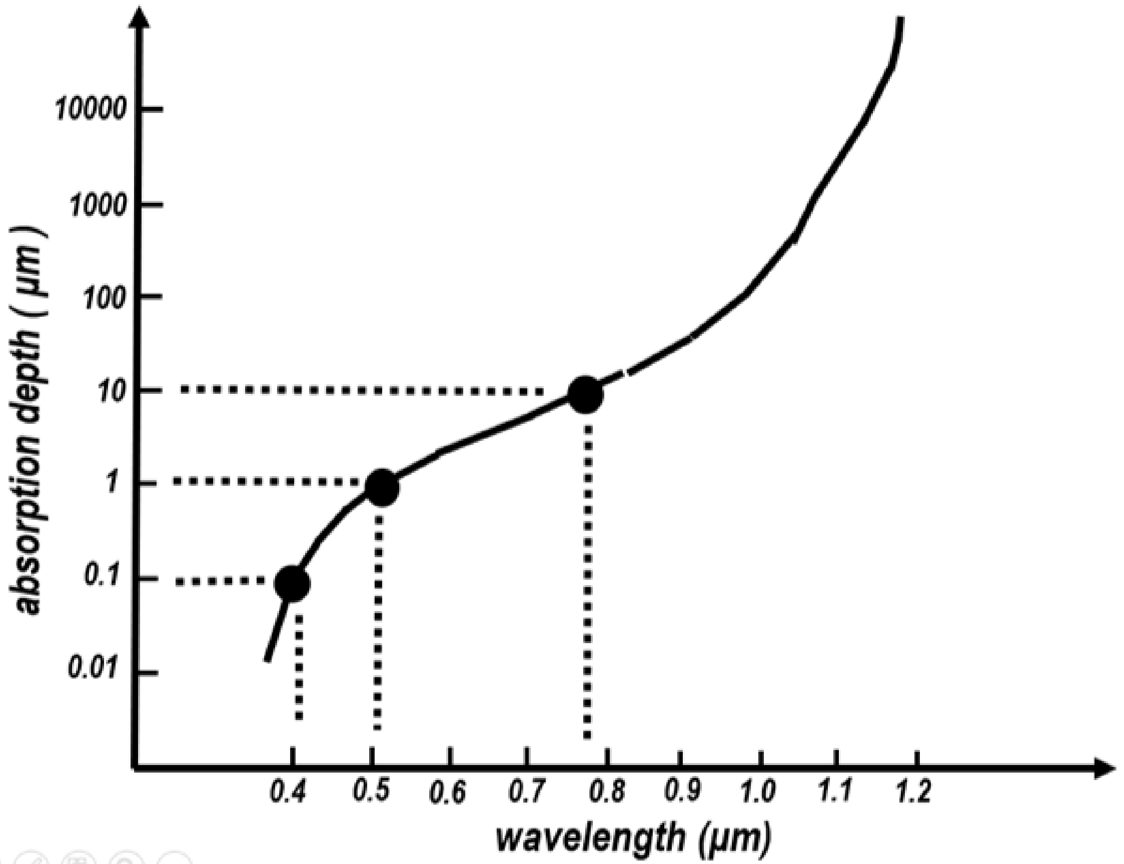
Yoshiaki. Hagiwara, Japanese Patent Applications JPA 1975-127647, JPA 1975-127647 and JPA 1975-134985.

# 8 Double Junction Photo Transistor type Solar Cell

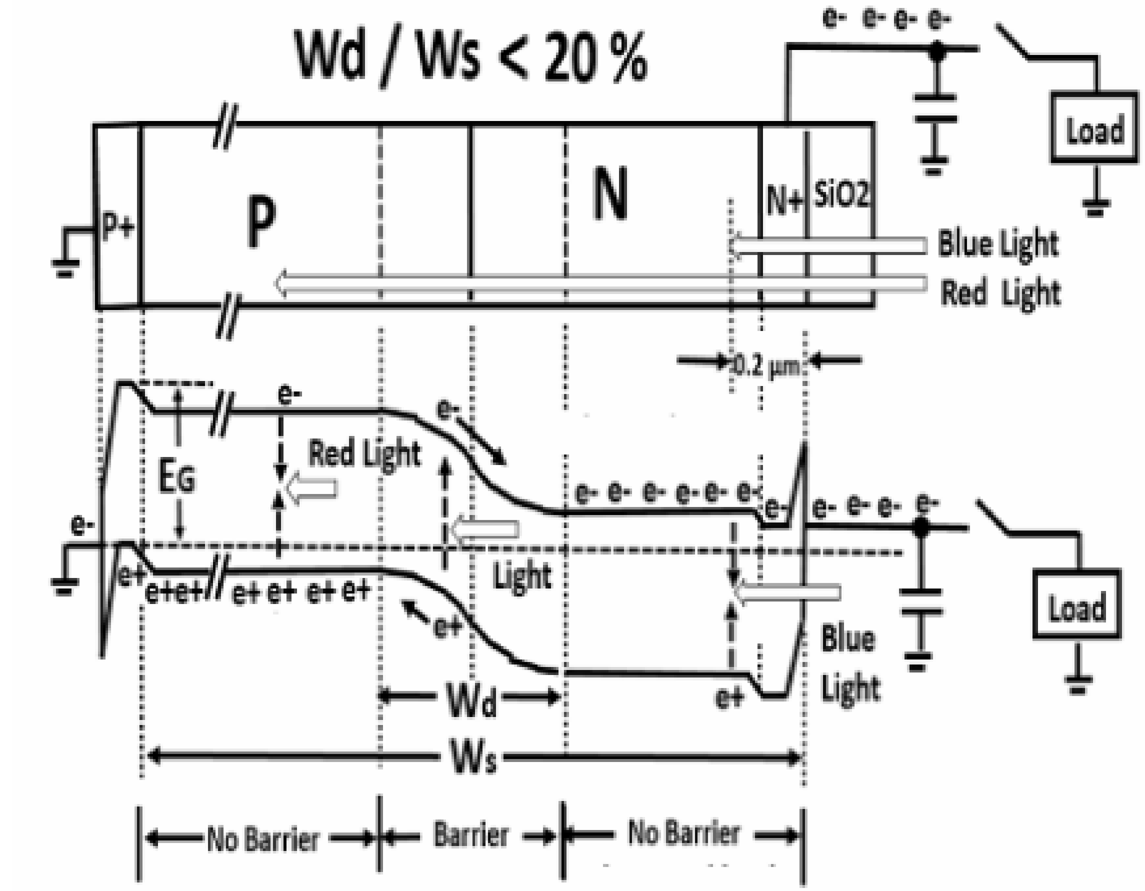
And the 60% efficiency solar cell may not be a dream if all of the photo electron and hole pairs are instantly separated by the presence of an electric filed and prevented from being recombined again completely.



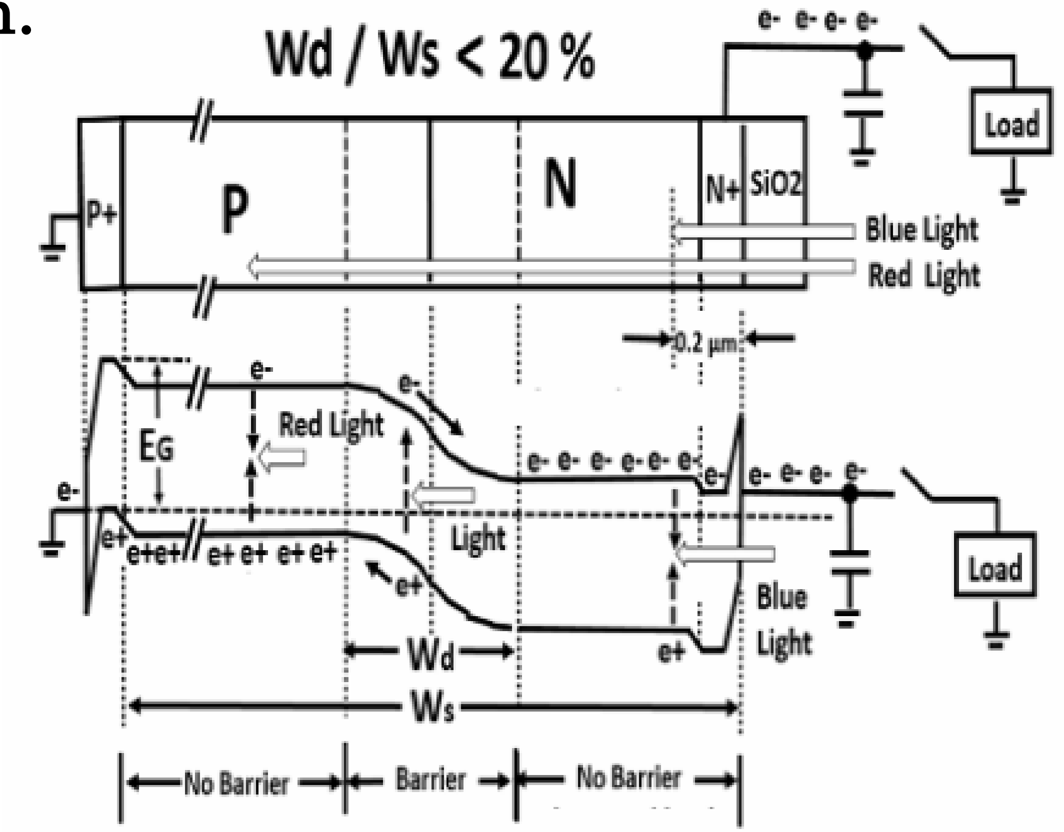
# 8 Double Junction Photo Transistor type Solar Cell

Since the surface floating N+N region with no electric field has flat potential with stored photo electron charges, electron hole pairs at the surface cannot be separated and do not contribute to the quantum efficiency.



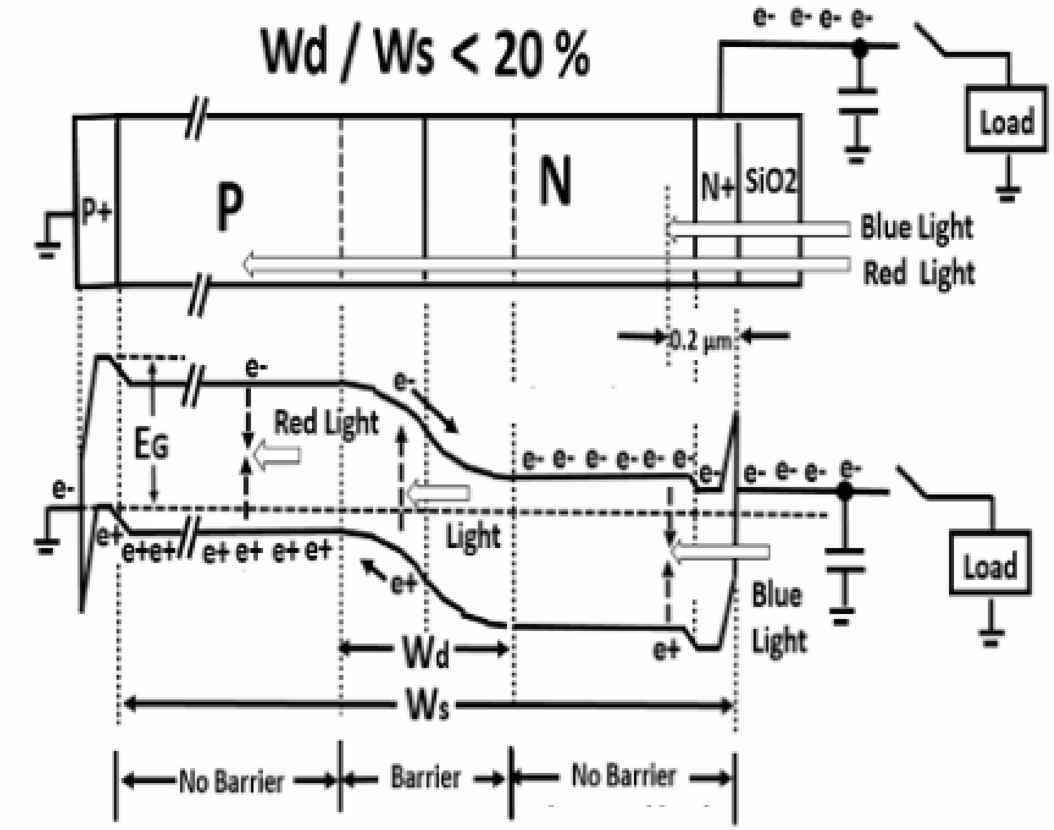
# 8 Double Junction Photo Transistor type Solar Cell

The short wave length blue light cannot penetrate silicon crystal more than 0.2 μm in depth. Most of the sun light energy is concentrated in the short wave blue light spectrum reaching only the floating N+ silicon surface vicinity of 0.2 micro meter in depth.



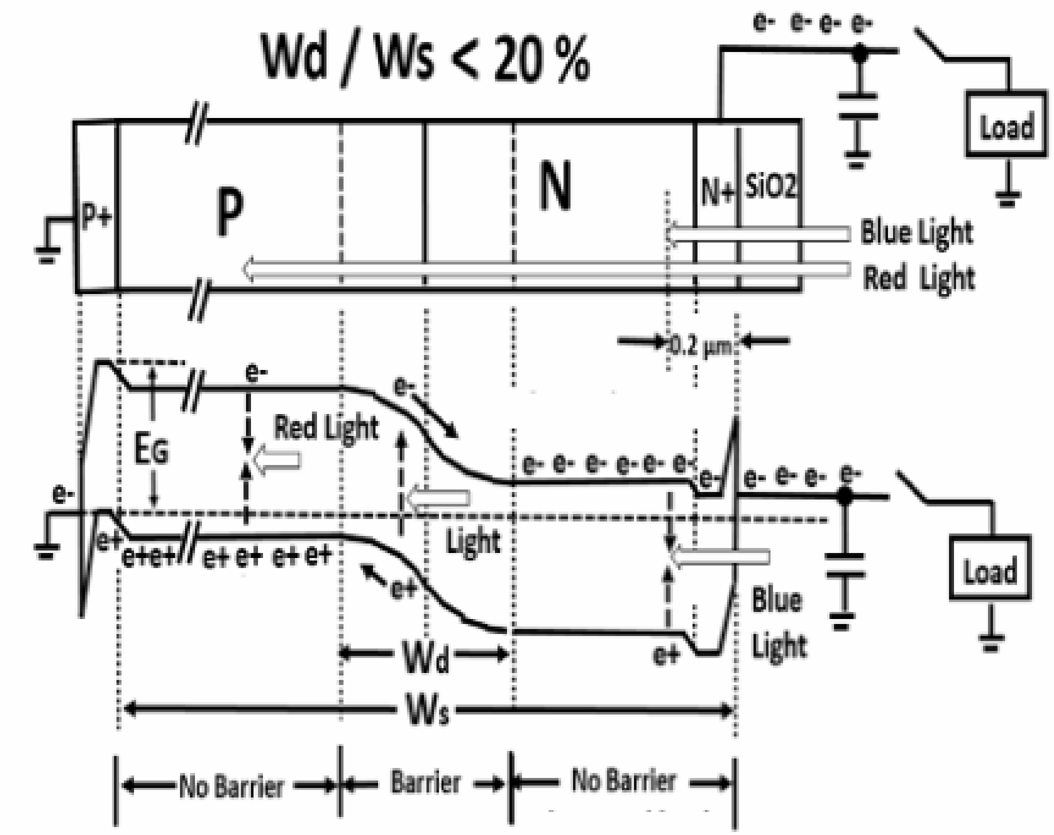
# 8 Double Junction Photo Transistor type Solar Cell

In conventional the N+P single junction type solar cells, the N+P junction depletion region width Wd is very narrow.



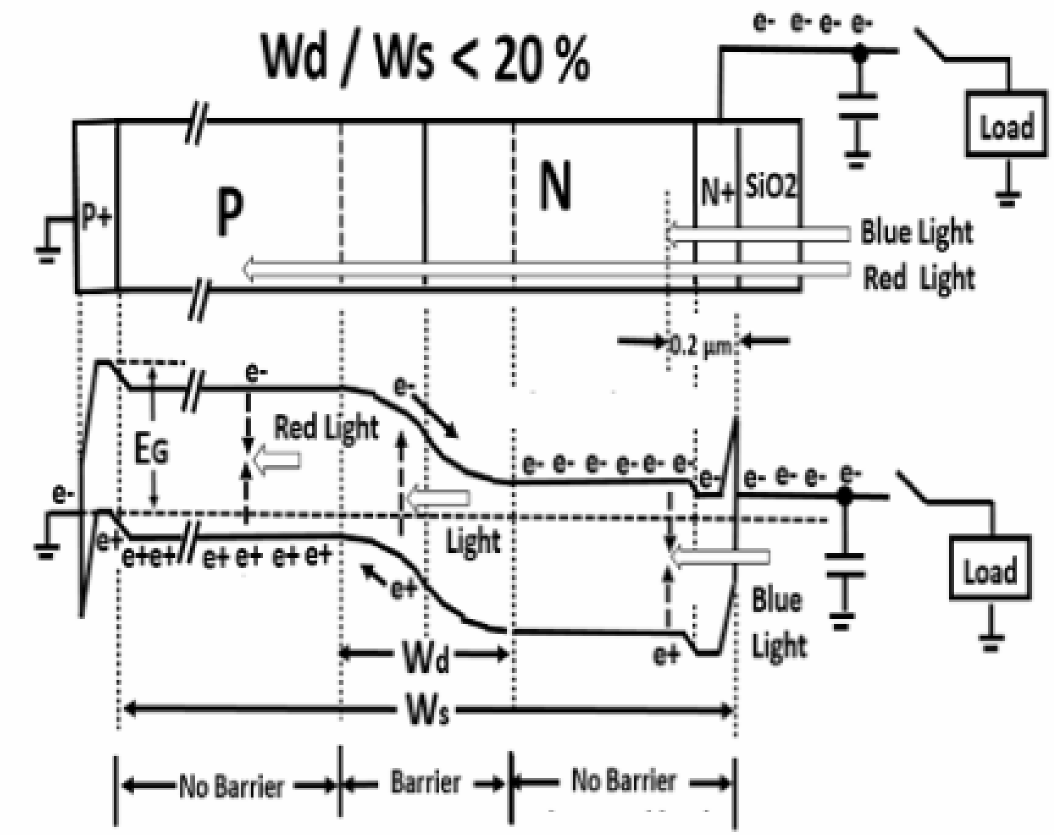
# 8 Double Junction Photo Transistor type Solar Cell

The large portion of the surface portion of the floating N+ region is used as the photo electron storage region which forms the sea of the photo electrons, with a flat photo electron sea level with no barrier electric field .



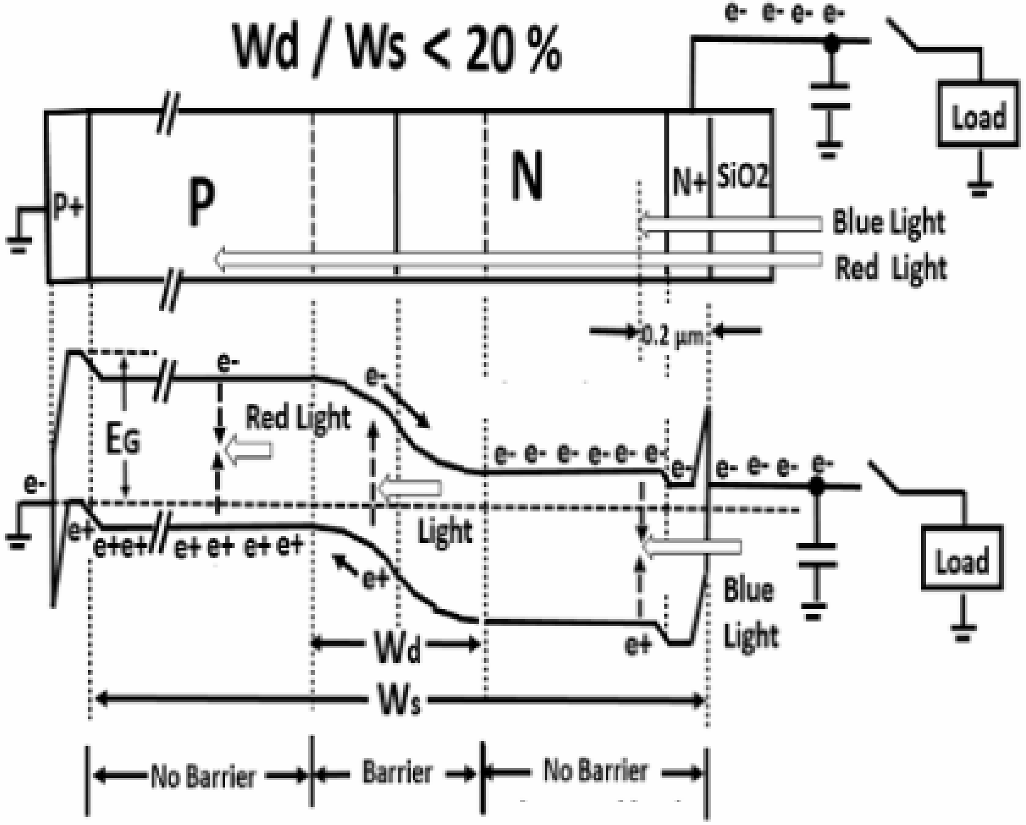
# 8 Double Junction Photo Transistor type Solar Cell

Most of the electron hole pairs generated at the silicon surface are recombined and do not contribute to the solar cell quantum efficiency.



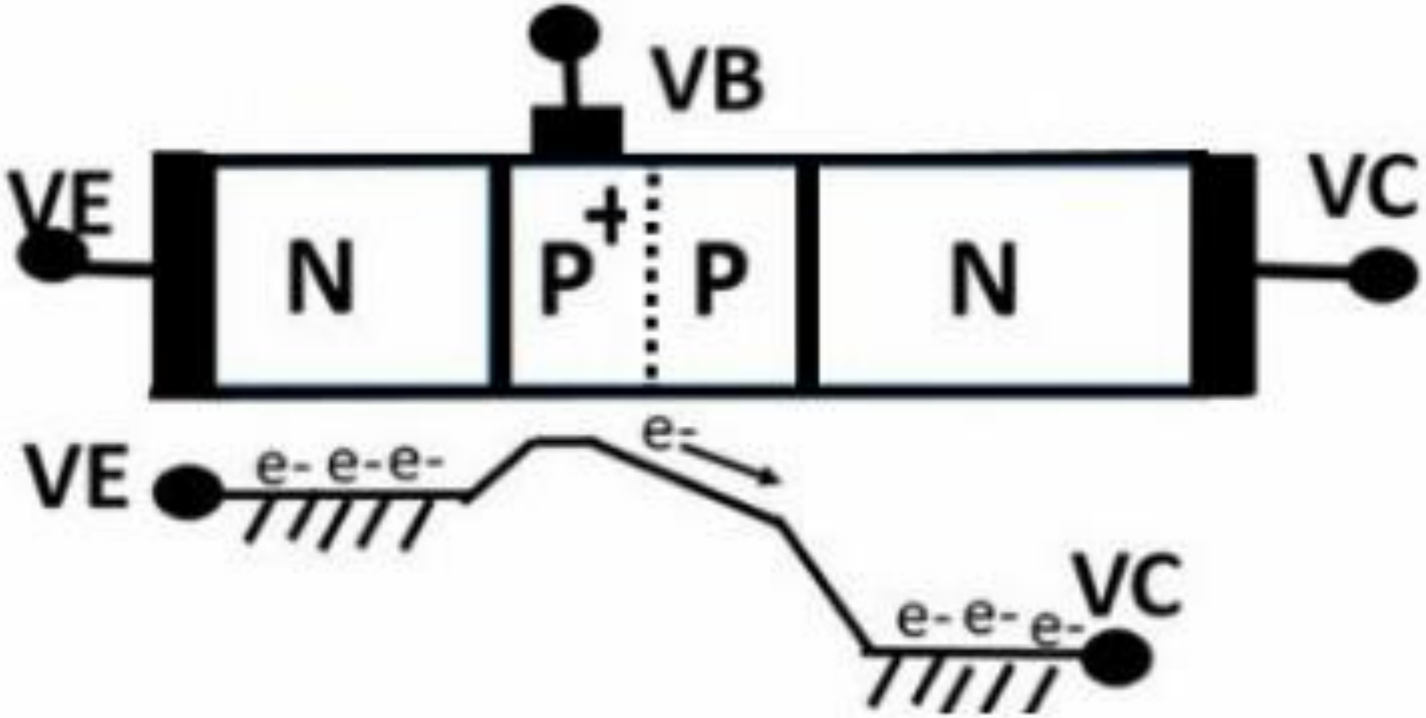
## 8 Double Junction Photo Transistor type Solar Cell

Barrier electric field is needed to separate the photo electron and hole pairs in solar cells. There are two methods to create barrier electric field. One approach is to use the PN junction depletion region.



# 8 Double Junction Photo Transistor type Solar Cell

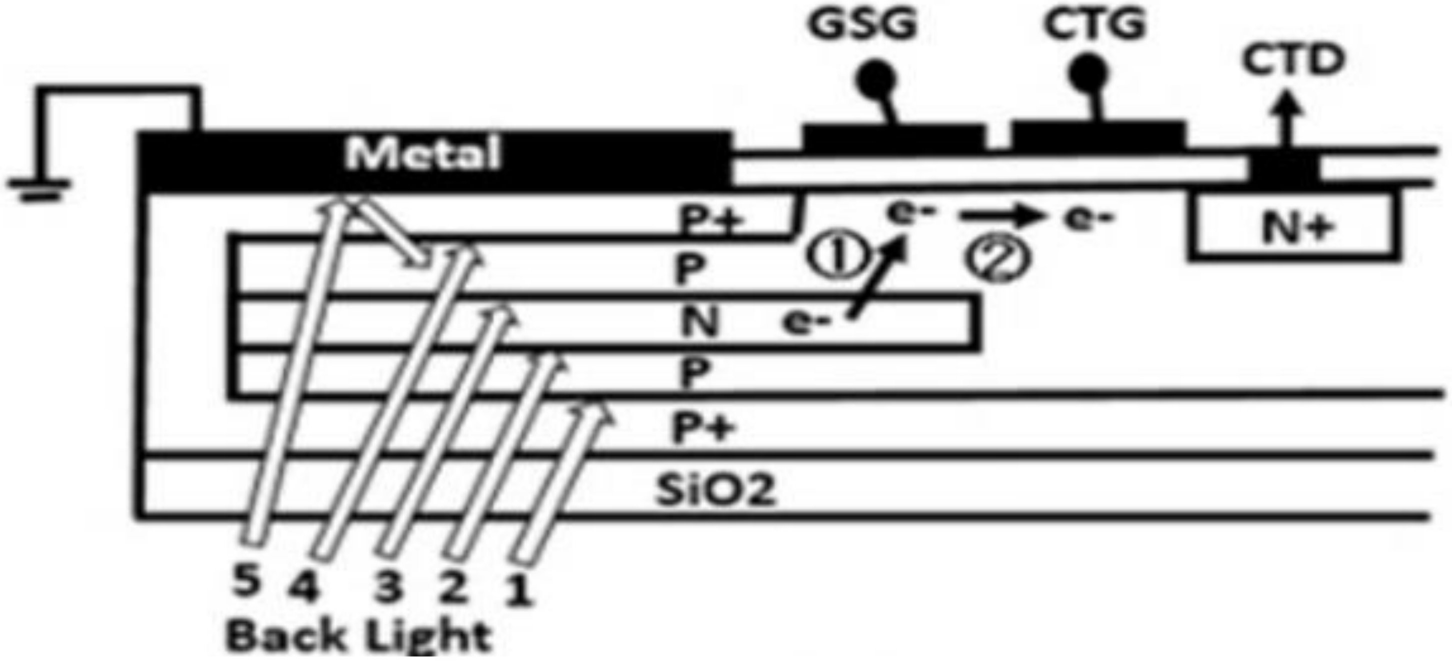
The second approach utilizes the principle applied in a drift field bipolar transistor base region with the P+P barrier electric field.




Drift Field Bipolar Transistor with P+P Barrier Electric Field

## 8 Double Junction Photo Transistor type Solar Cell

The second approach has been applied also in the form of the surface Pinned P+P Hole Accumulation Photodiode (HAD) for highly light sensitive imager sensors.

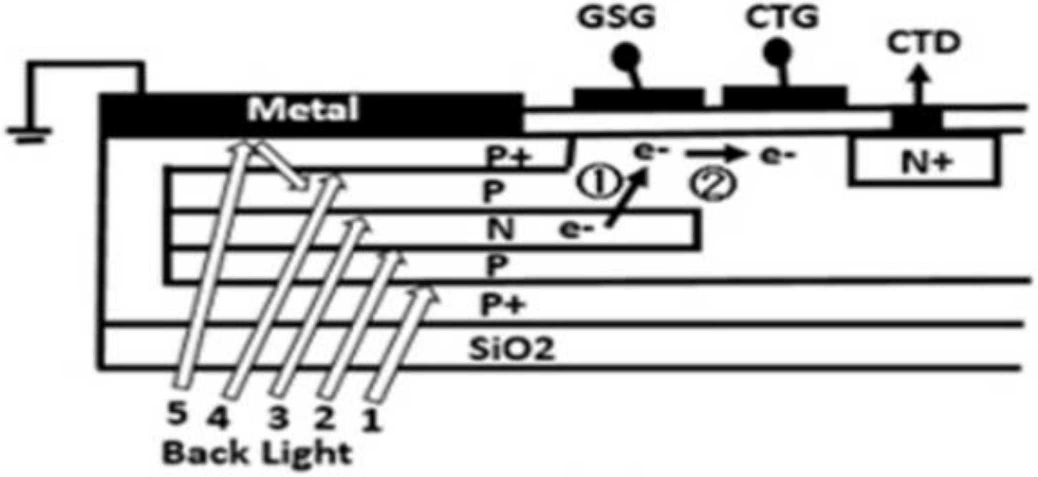



P+PN+PP+ type Back Light Illumination CMOS Imager

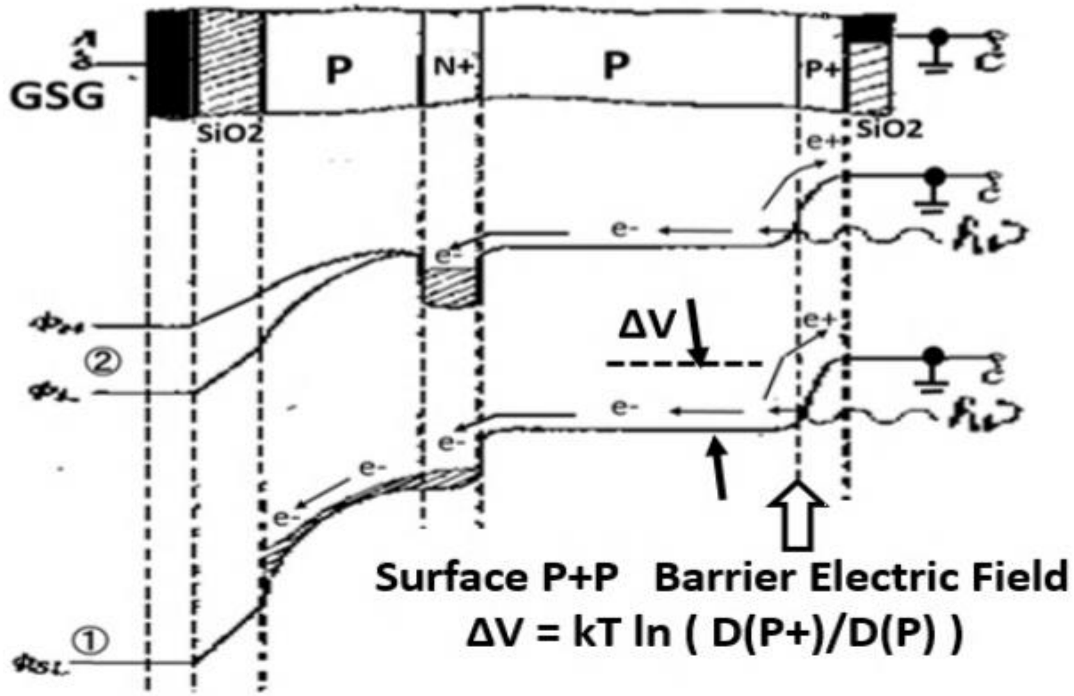
Yoshiaki . Hagiwara, " Multichip CMOS Image Sensor Structure for Flash Image Acquisition ", IEEE 3DIC2019 conference in Sendai, Japan, Oct 2019

# 8 Double Junction Photo Transistor type Solar Cell

The cross sectional view of a typical back light illuminated CMOS image sensor in the global shutter scheme with an MOS gate buffer memory (GSG) is shown with the surface Pinned P+P Hole Accumulation Photodiode (HAD) widely used now for highly light sensitive imager sensors.

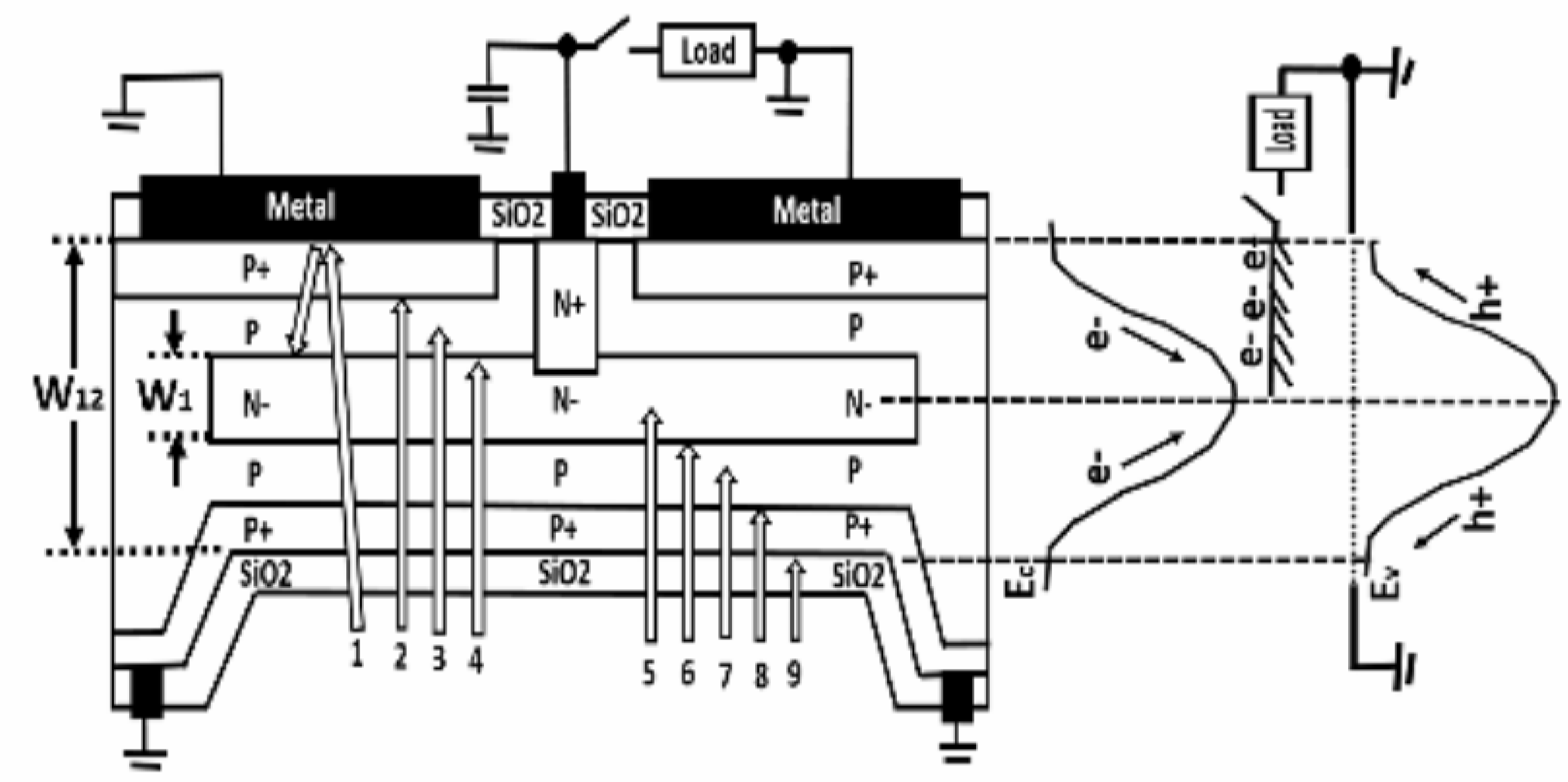



P+PN+PP+ type Back Light Illumination CMOS Imager



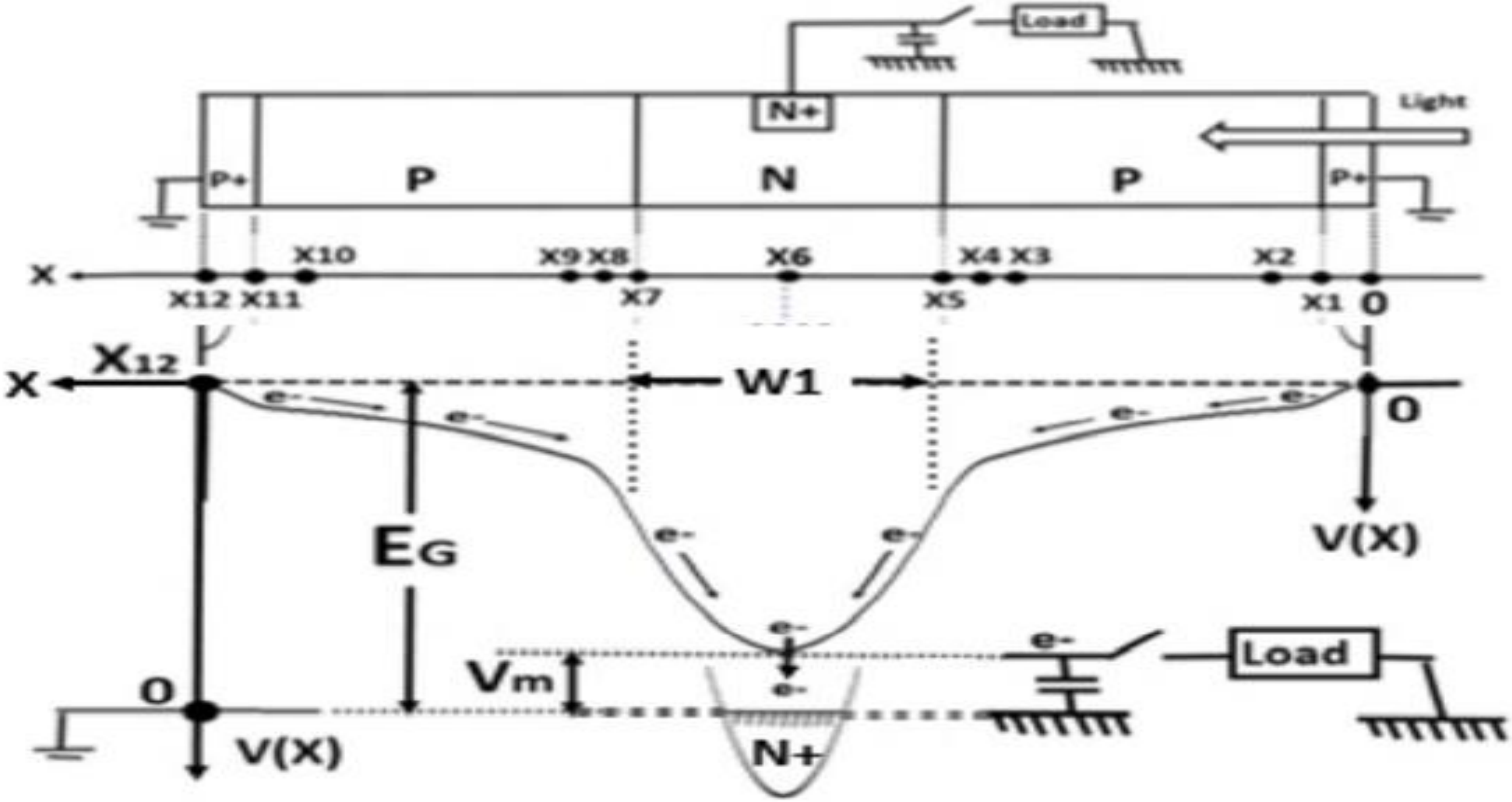

Yoshiaki . Hagiwara, " Multichip CMOS Image Sensor Structure for Flash Image Acquisition ", IEEE 3DIC2019 conference in Sendai, Japan, Oct 2019

# A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell



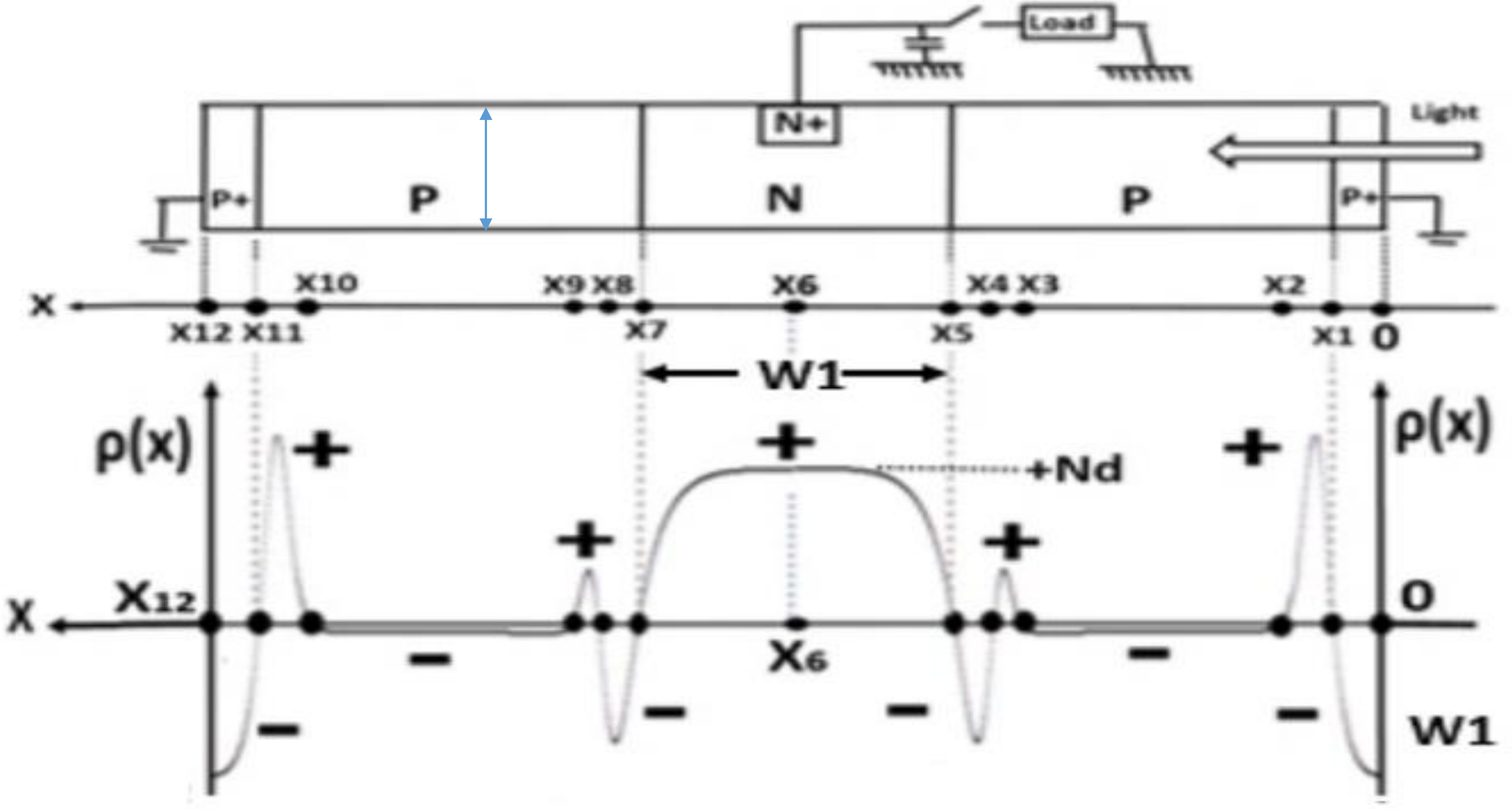
A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

Poisson equation $dV(x) / dx = \rho(x) / \varepsilon si$ was solved numerically for the electron potential V(x).



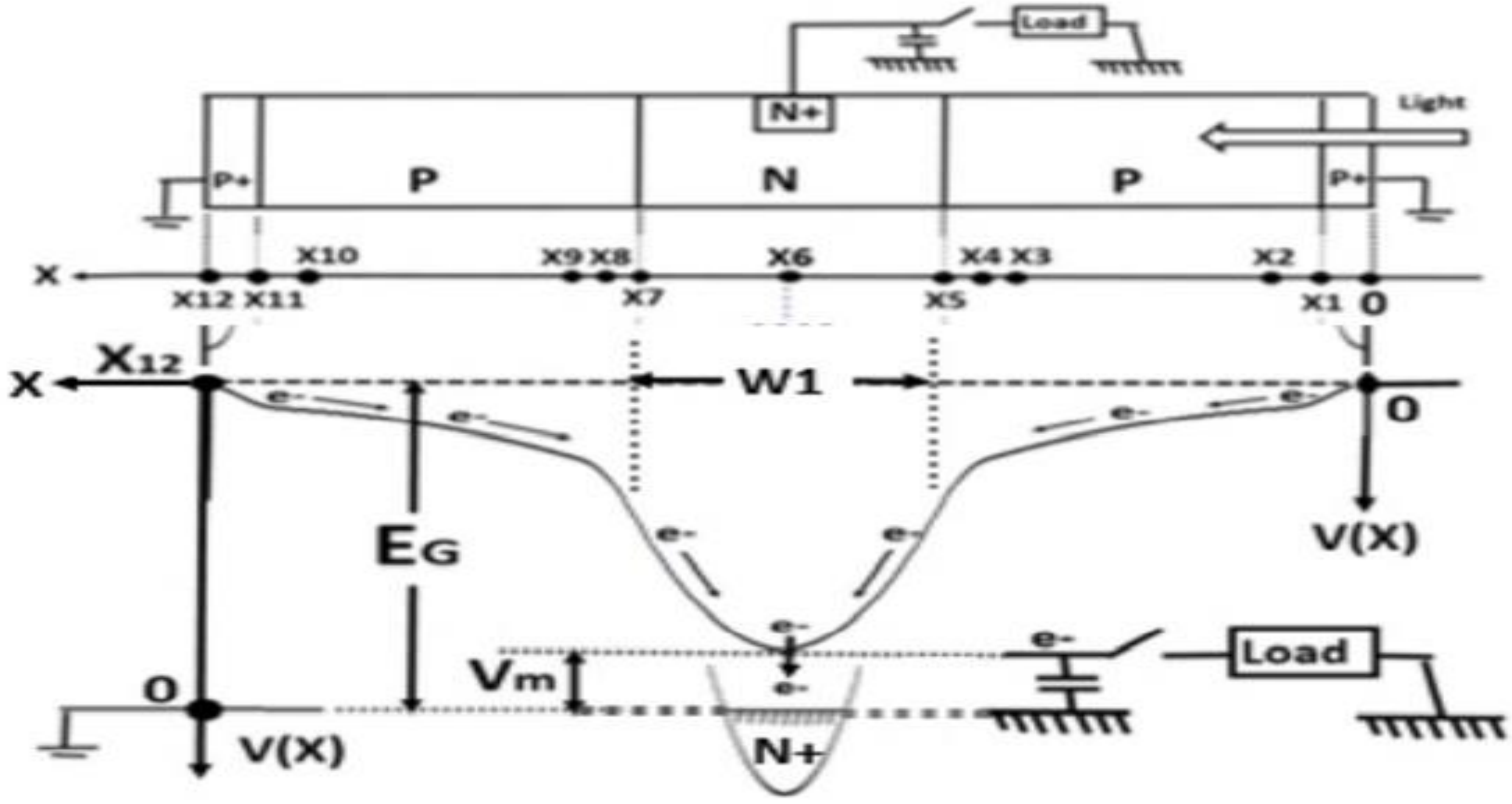
A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

The space charge polarization $\rho(x) = D(x) - P(x)$ is also calculated where P(x) is the hole carrier concentration.



A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

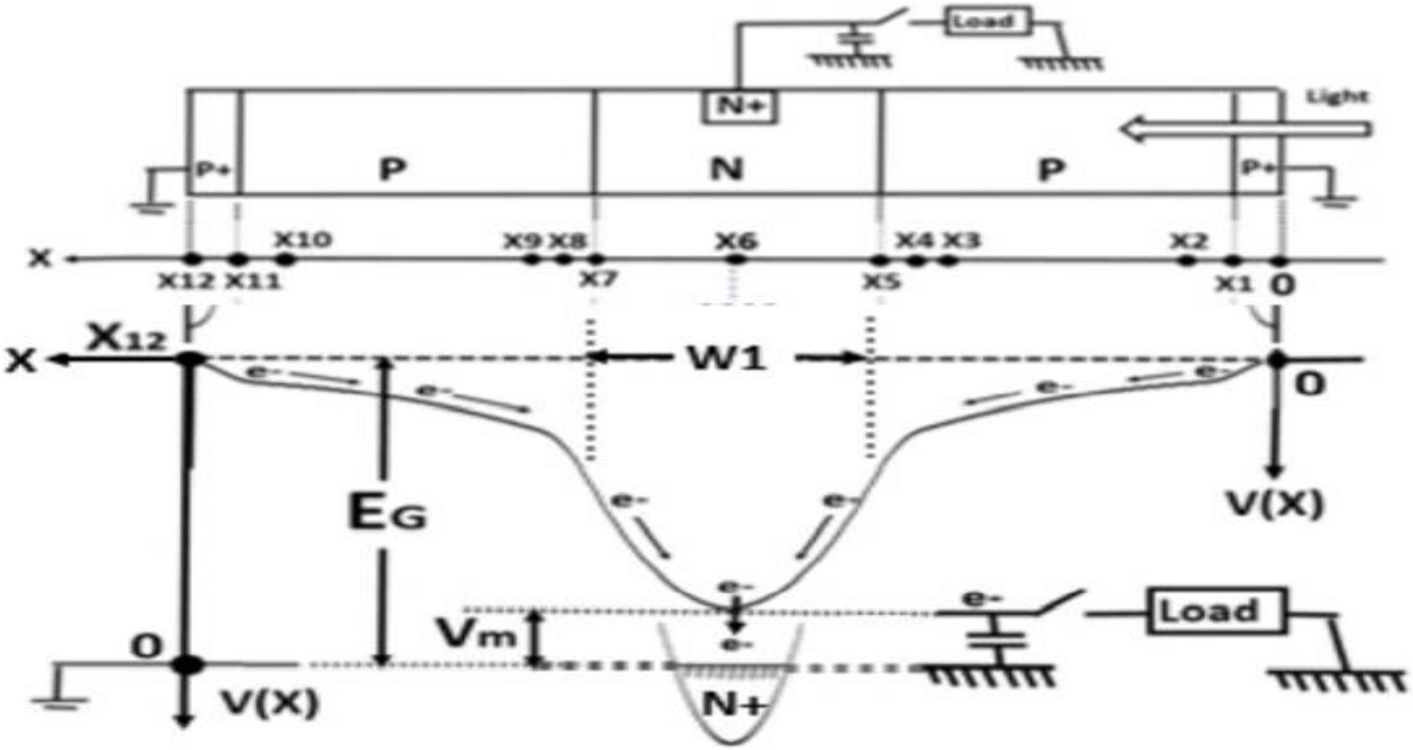
In this case study, the surface P+P Hole Accumulation Photodiode (HAD) was assumed to have a smoothly varying shape of a Gaussian function defined here as Gaus (X) = exp ( $-x^2$ ) .



A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

For the P+P double surface ion implantation process of our case study we set with $R_s \ll R_a$ and $N_s \gg N_A$.

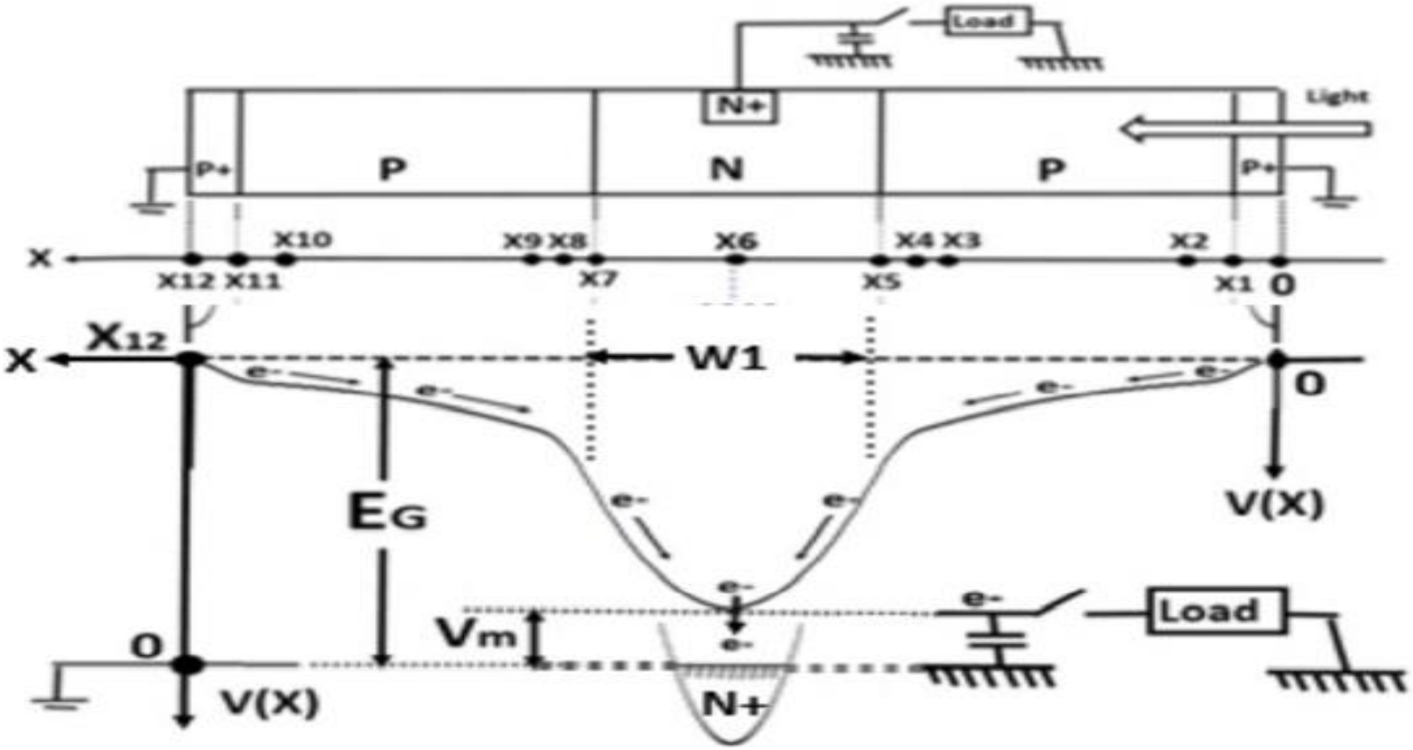
$$D_s(x) = (N_s - N_A)\, Gaus(x / R_s) + N_A\, Gaus(x / R_a) .$$



The total doping is then given as

$$D(x) = Ds(x) + Ds\,(\,Xd - x\,)\ - Nd$$

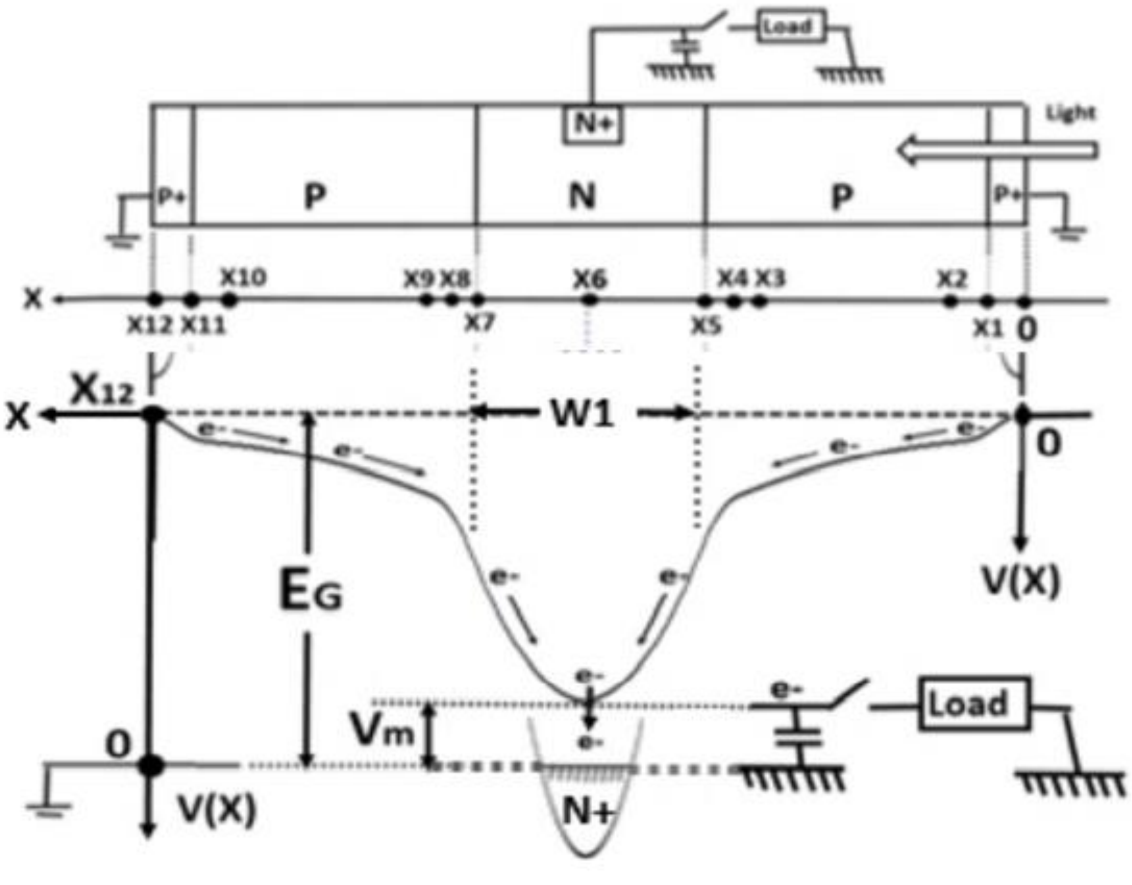
where Nd is the N-type original substrate doping level.



A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

If the surface P+P is a uniform abrupt doping level Ns and $N_A$,
the surface barrier potential drop $V_{bar}$ can be obtained as

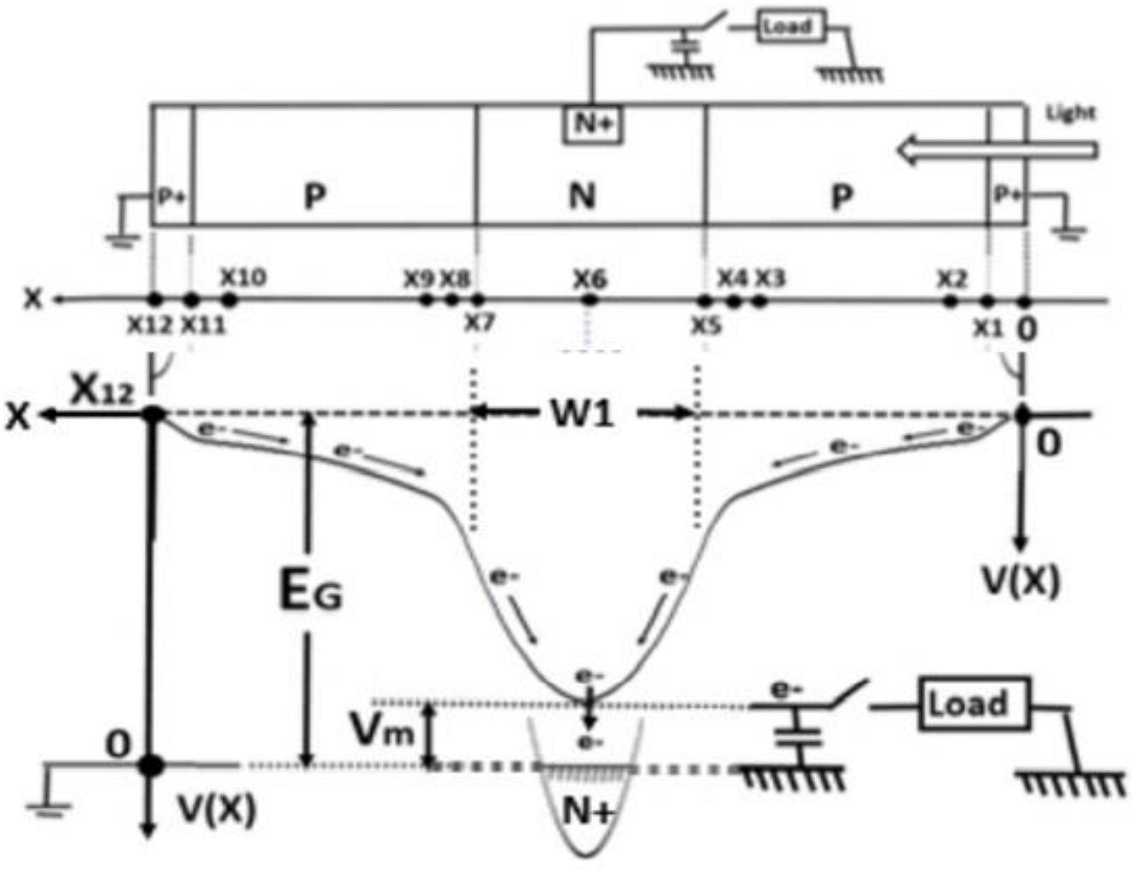
$$V_{bar} = kT \ln(N_s/N_A) = 0.0776\,\text{eV} \quad \text{with} \quad kT = 0.0259\,\text{eV}.$$



A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

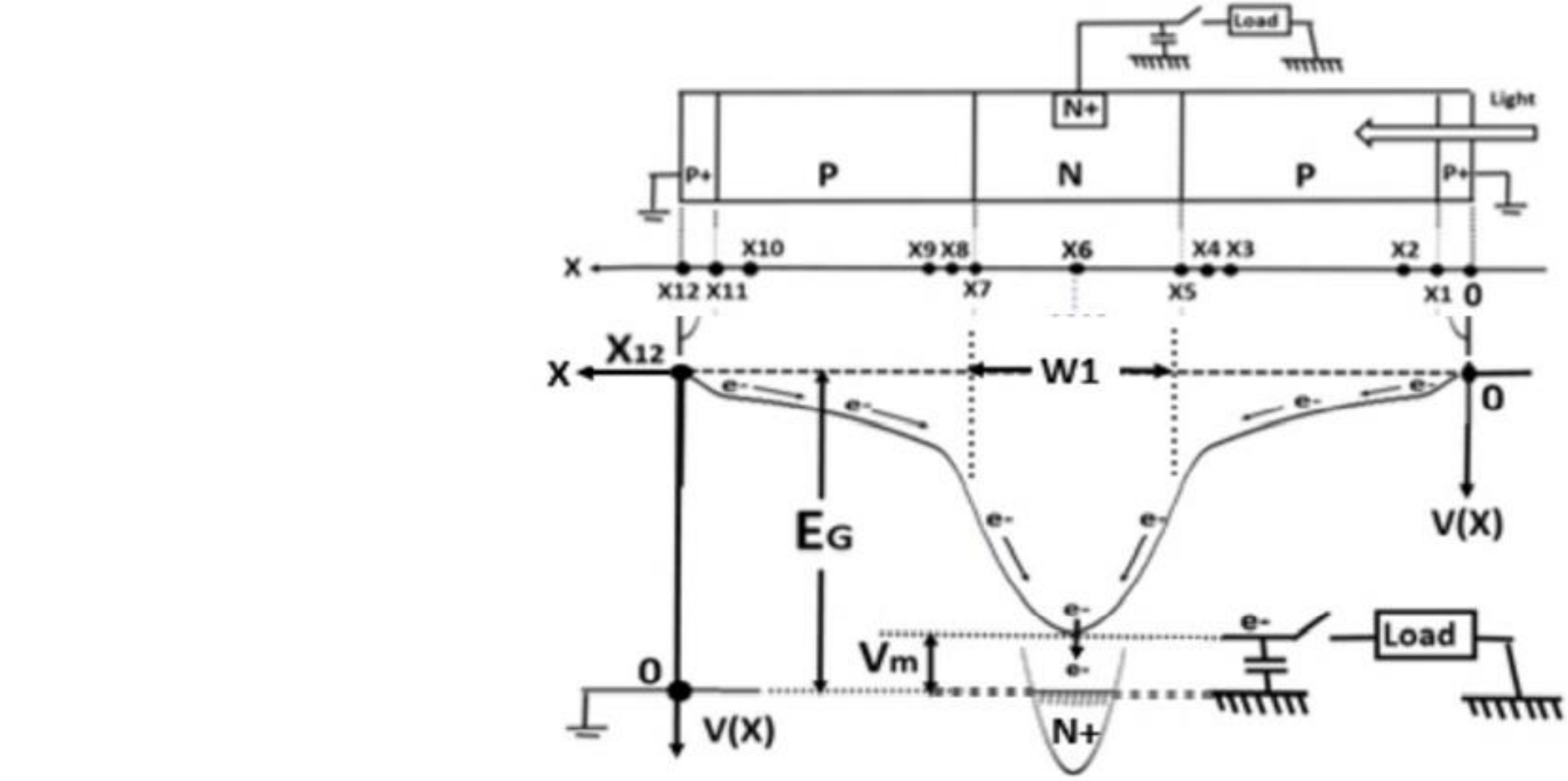
## Salient physical parameters were set as

$$N_d = 100 \ e\ \mu m^{-3},\ N_s = 1 \times 10^{5}\ e\ \mu m^{-3} \text{ and } N_A = 5 \times 10^{7}\ e\ \mu m^{-3}$$



# A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

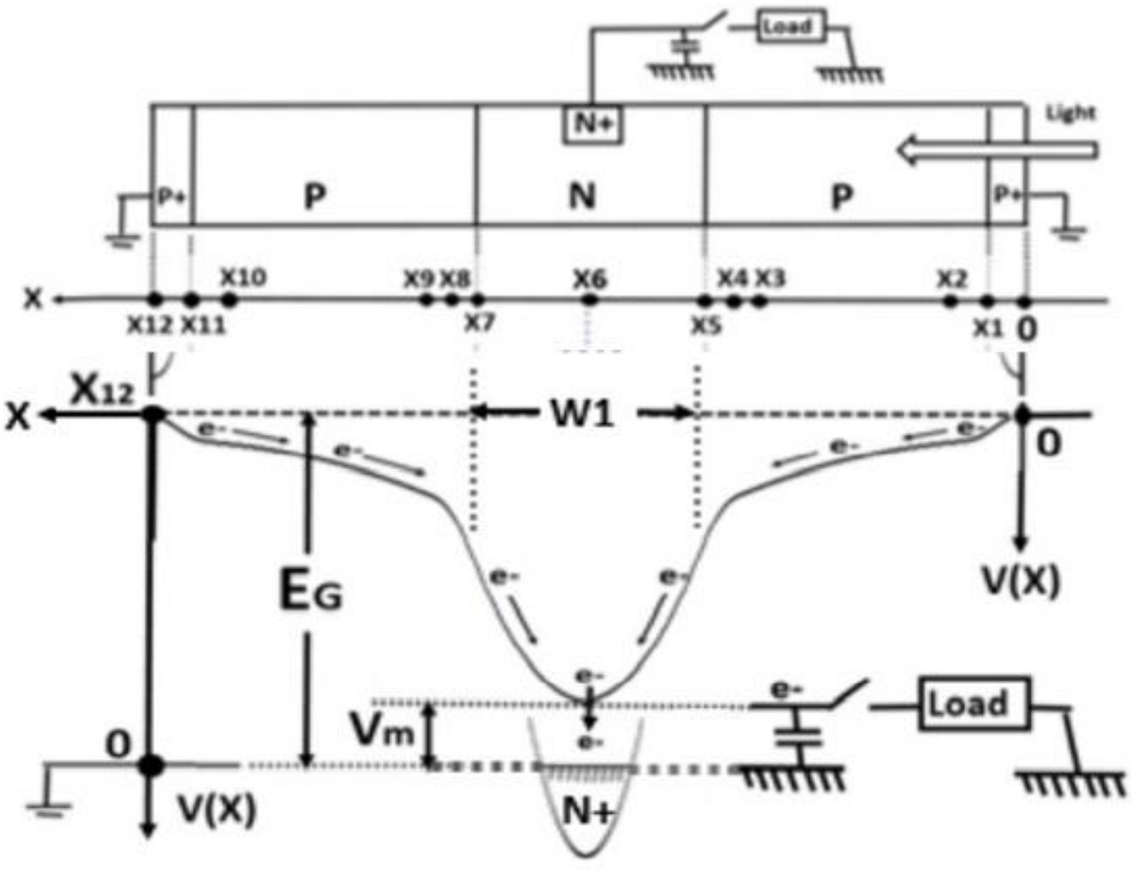
## The ion implantation parameters are chosen as Rs = 0.57 µm and Ra = 2.5 µm with the width of the device X12 = 20 µm.



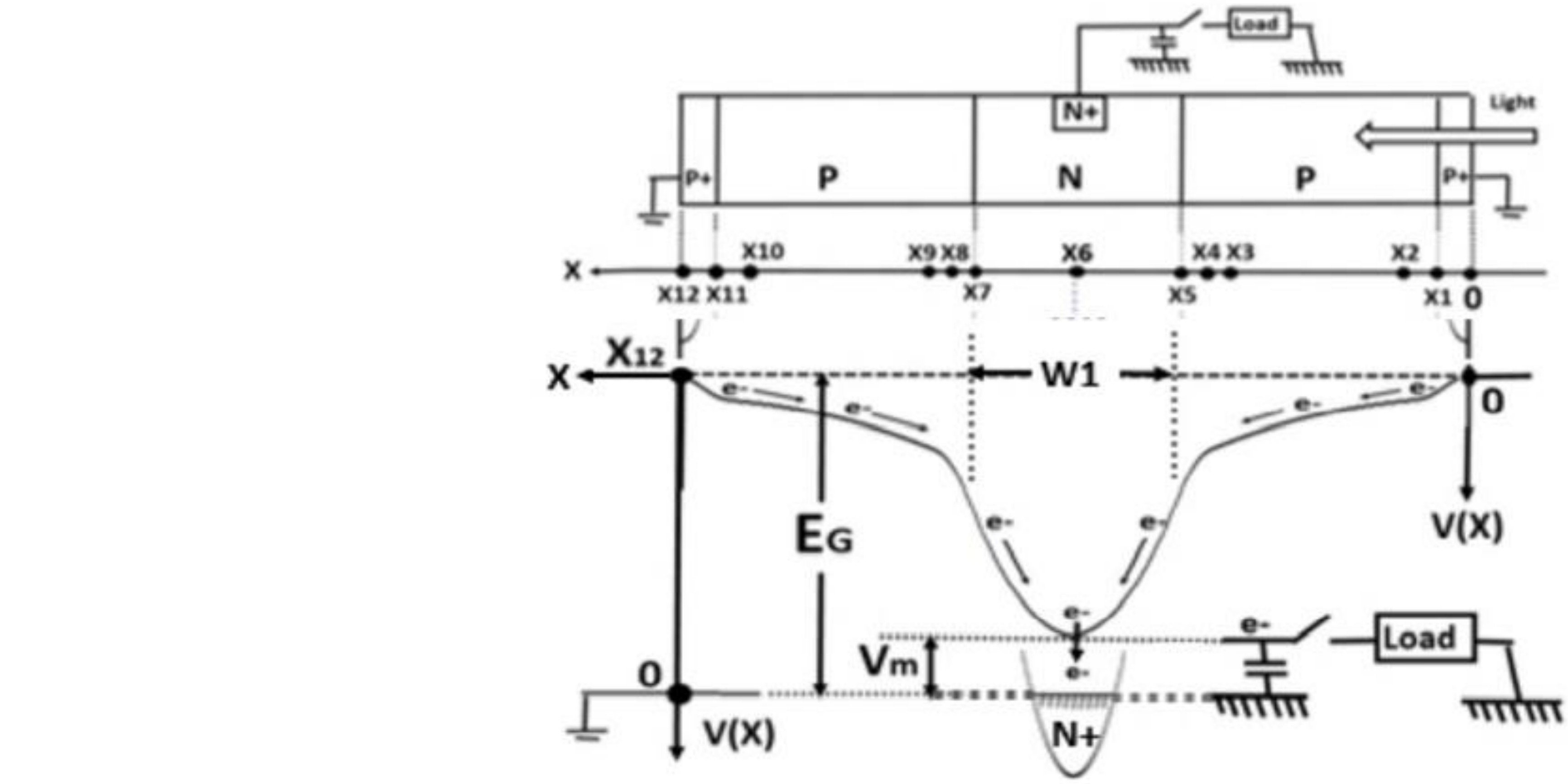
A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

## The difference of the hole potential Ve(x) and the electron potential Vh(x) is the silicon band gap EG.

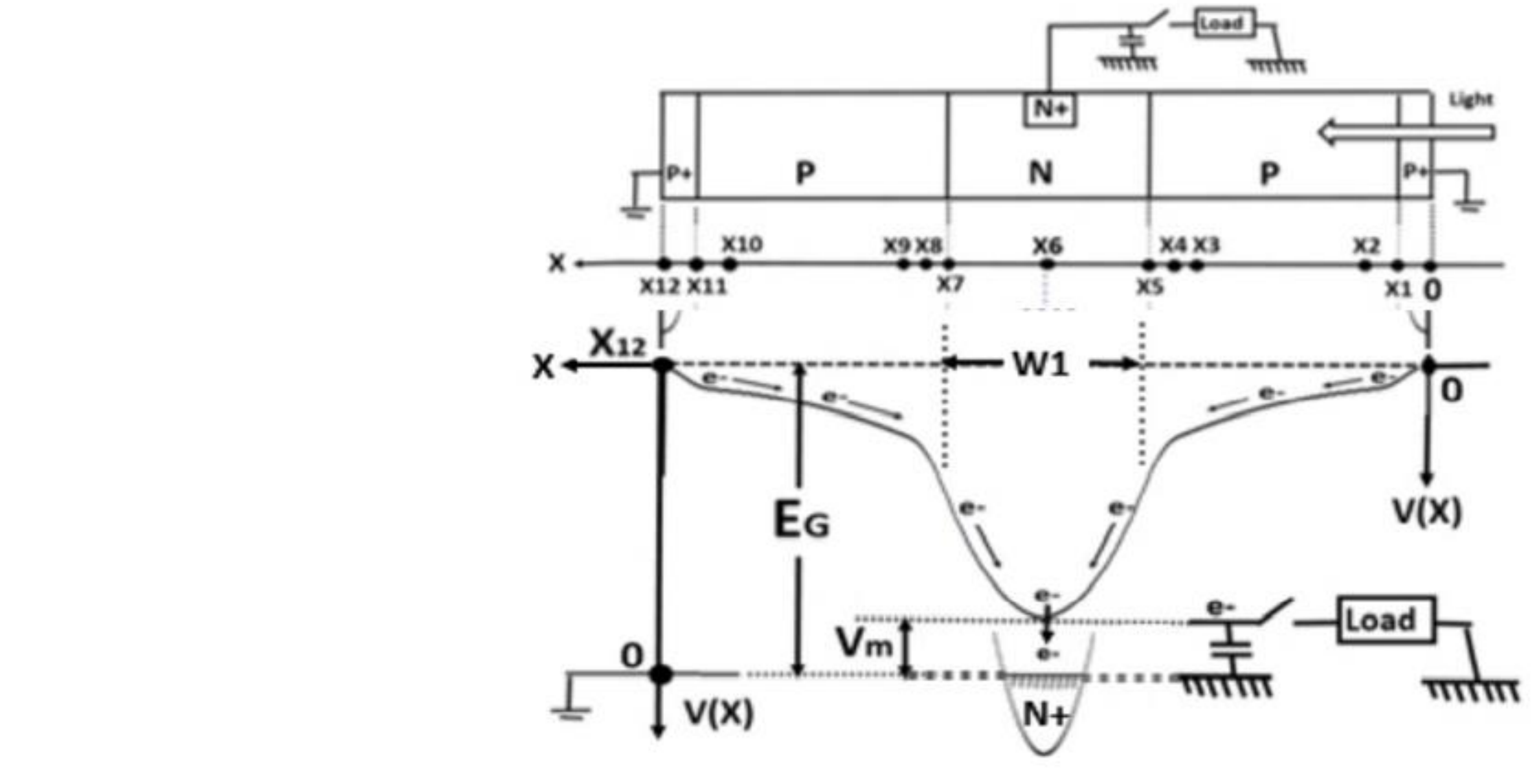
$$Vh(x) - Ve(x) = E_G.$$



Since the P+ regions in both side of the device are connected and pinned by the outside metal ground wire, the values of the hole potential Vh(x) at the both sides are defined as the ground level of 0 volt.

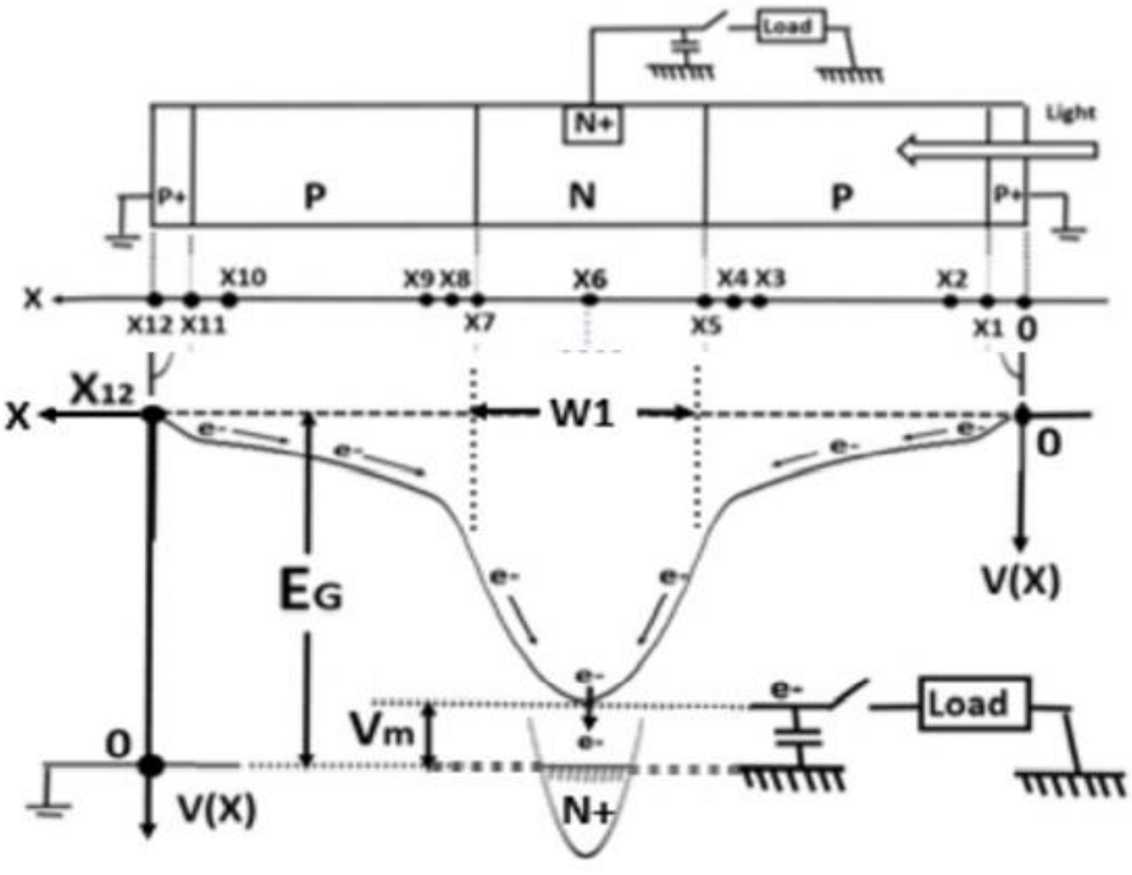


The curve shown in the figure is the electron potential Ve(x) for the photo electron charge carriers. Vh(x) = 0 V at the both edges while Ve(x) = – EG.

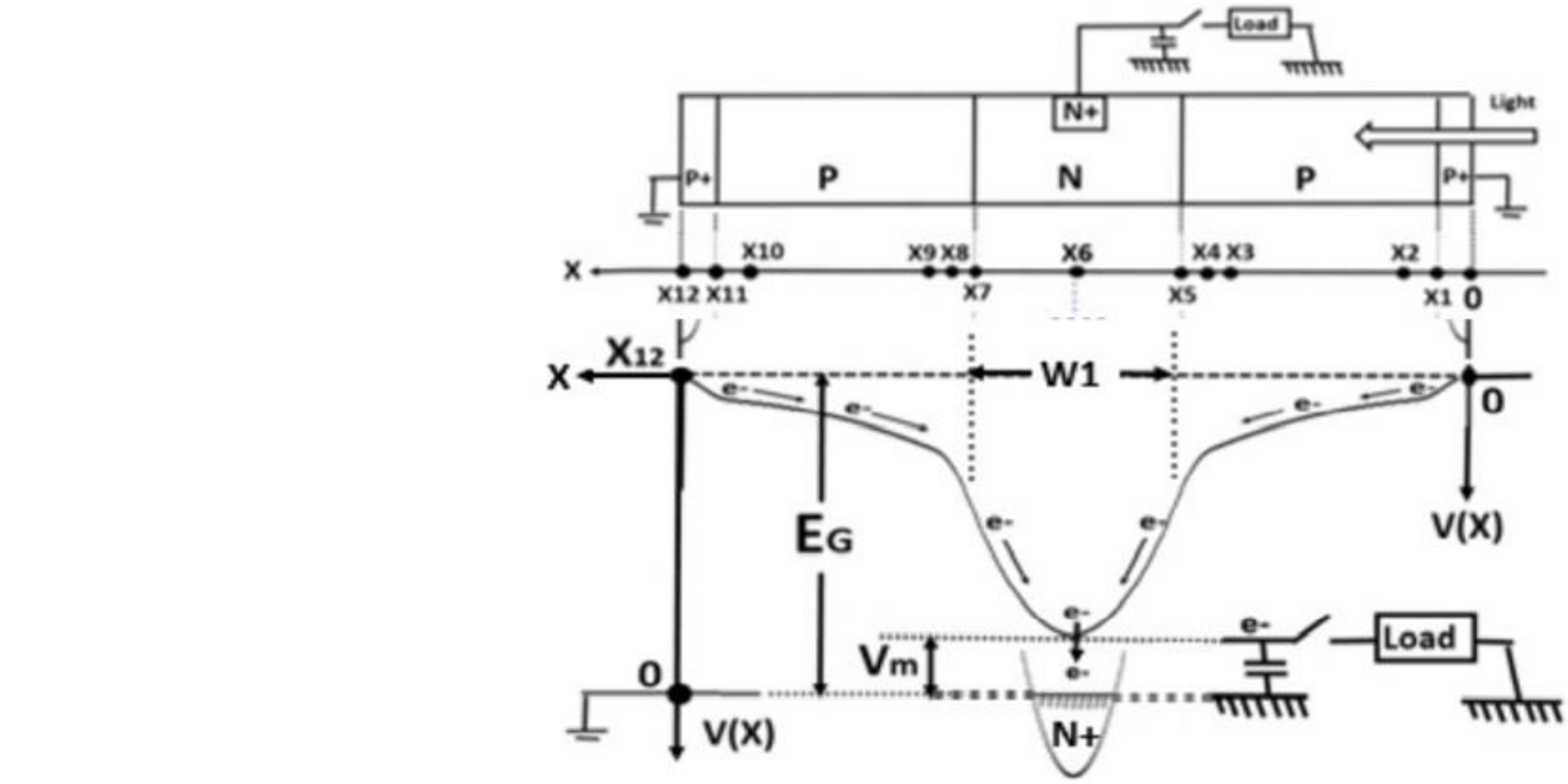


A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

The empty potential well is pinned and is given as Vm = – 0.203 eV. All the photo electrons are to be drained down into the center charge collecting and storage N+ region.

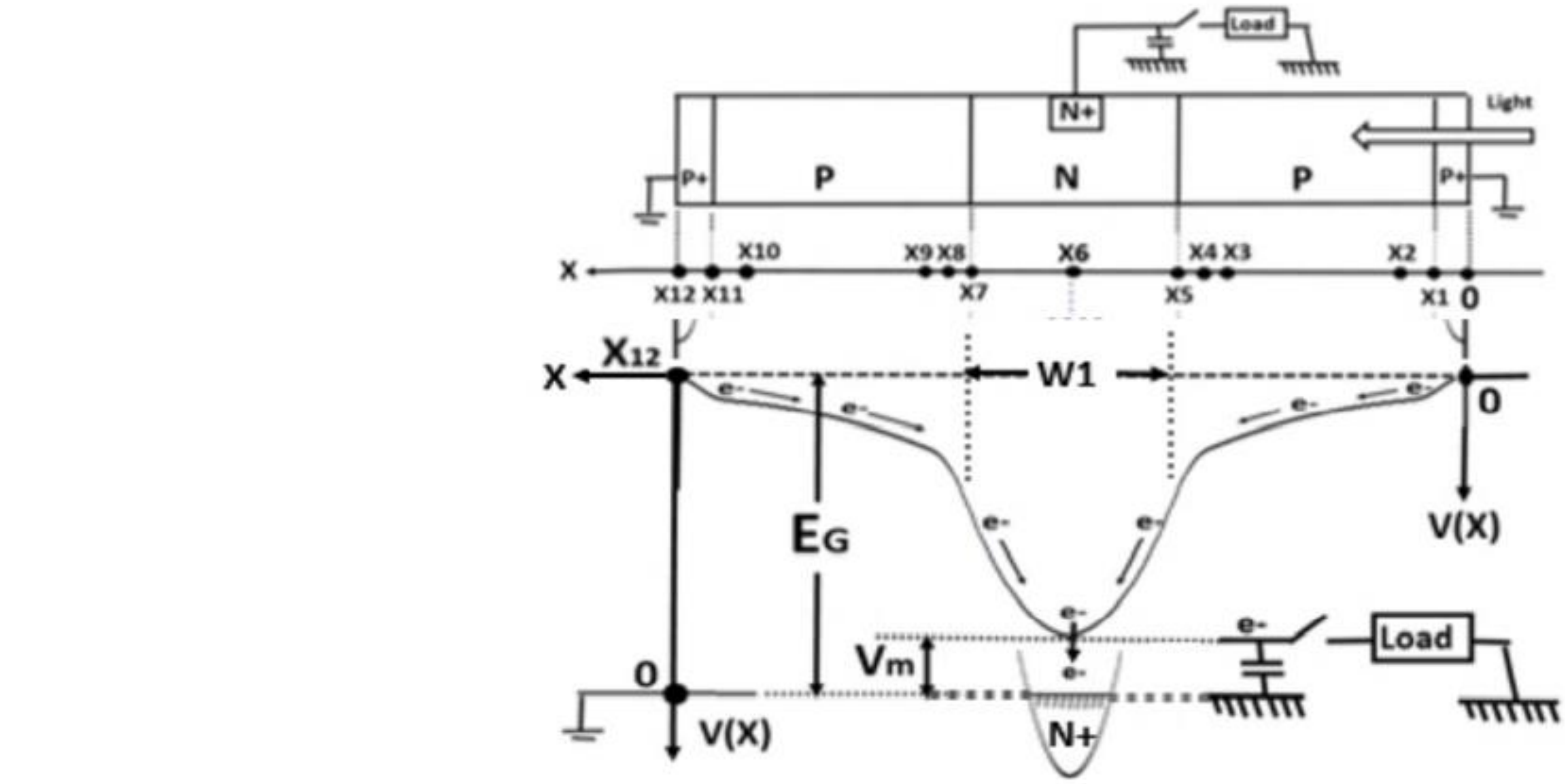


Other parameters obtained were X1= 0.828 µm, X2 = 1.726 µm, X3 = 6.315 µm, X4 = 6.705 µm and X5=7.292 µm.



A case study of a double junction P+PNPP+ Pinned Buried Photodiode type solar cell

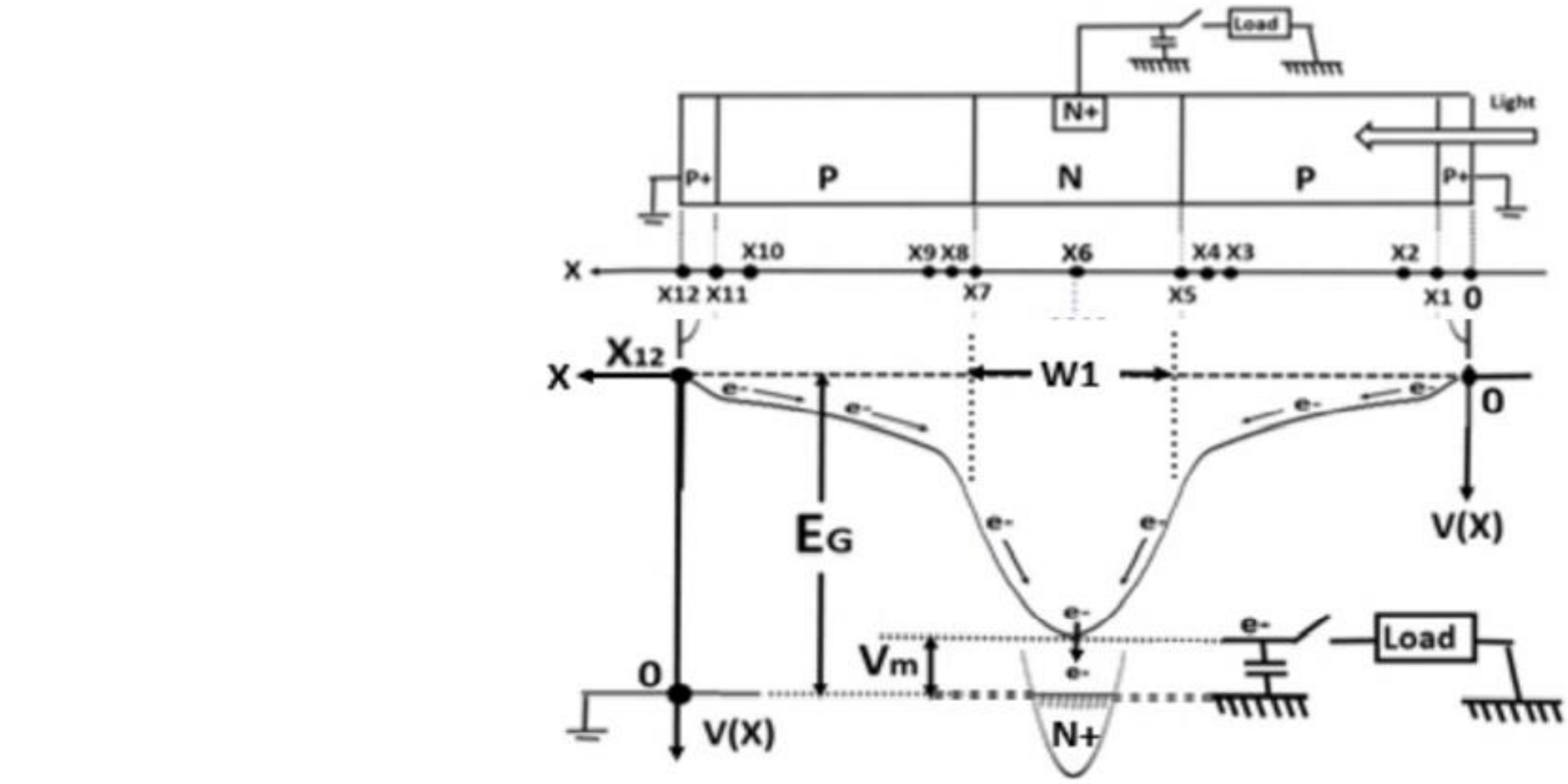
The buried N region width is given as W1 = X7 – X5 = 5.416 µm.
The charge capacity was computed as Qd = 459.5 e µm$^{-2}$.



The average doping level was then given as

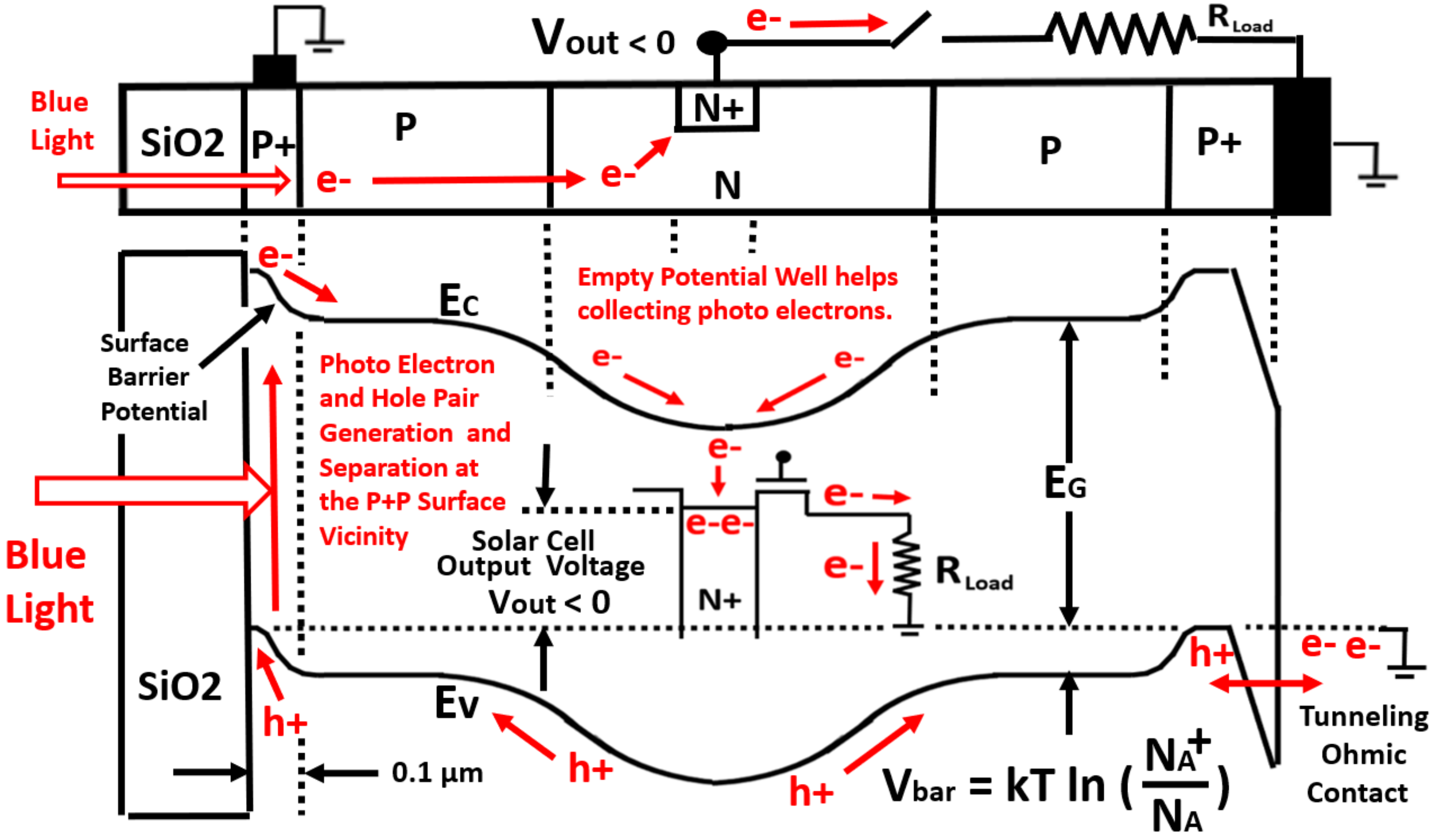
$$\langle Nd \rangle = Qd / W1 = 84.84 \text{ e } \mu m^{-3}$$

which is close to the initial N type substrate doping level $Nd = 80 \text{ e } \mu m^{-3}$.



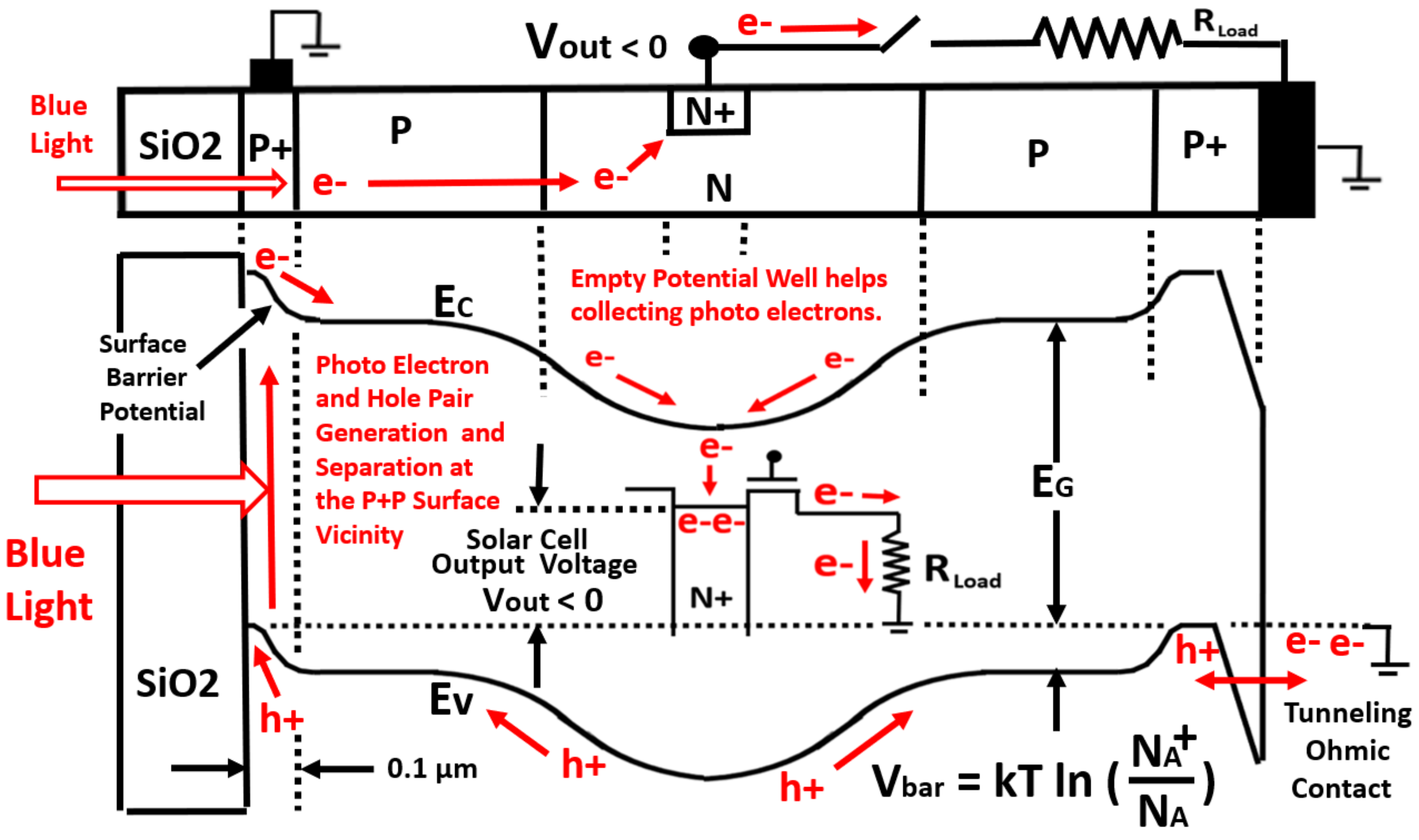
# 8 Double Junction Photo Transistor type Solar Cell

A conventional ion implantation gives a natural Gaussian P+P doping profile at the surface hole accumulation region which creates the barrier potential Vbar = kT ln ( $N_{A+}/N_A$) at the vicinity of the silicon surface.



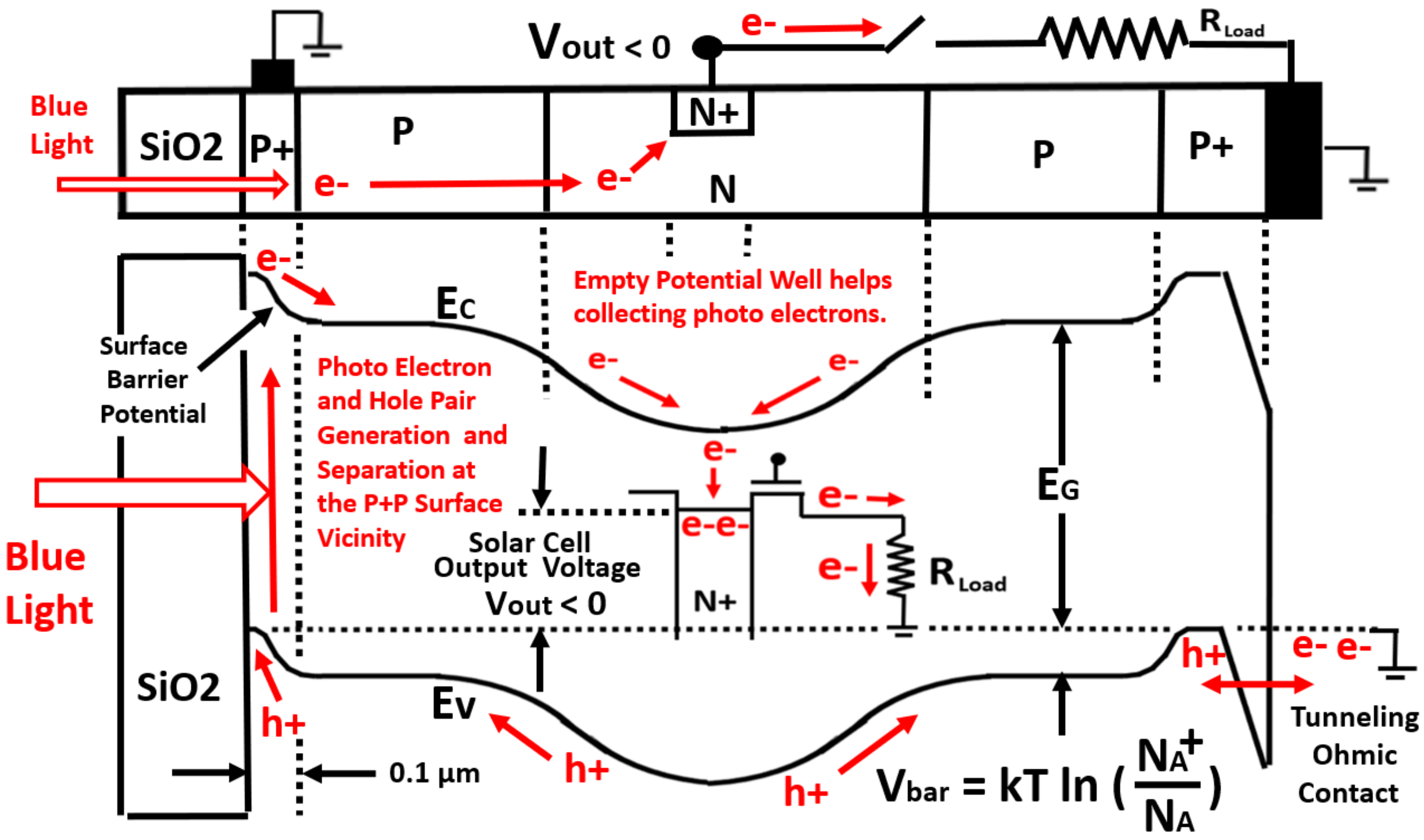
# 8 Double Junction Photo Transistor type Solar Cell

A high energy photon with very short wave length can be collected very effectively. The output voltage Vout of this P+PNPP+ double junction Pinned Photodiode type solar cell is less than the silicon band gap $E_G$ = 1.1 eV.



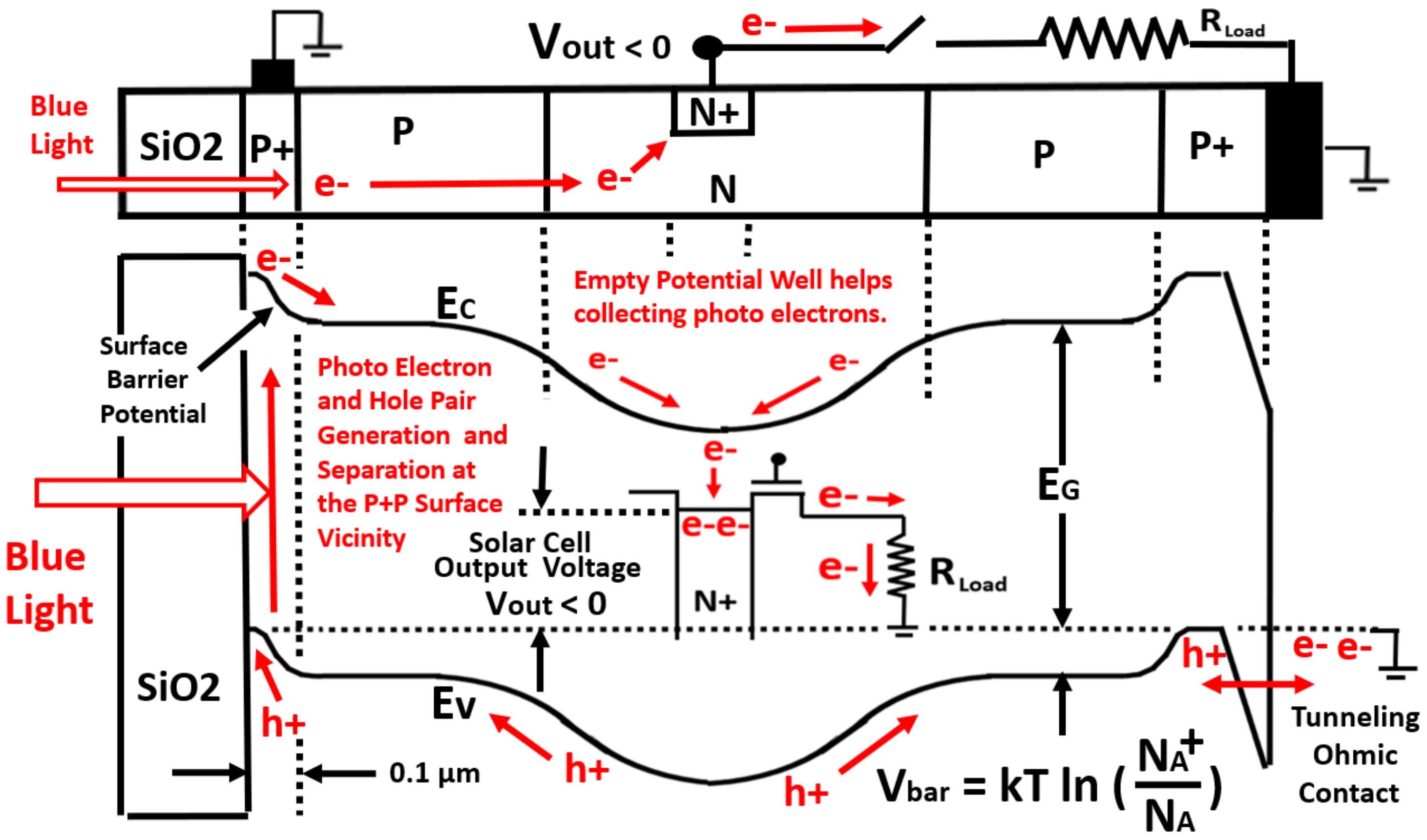
# 8 Double Junction Photo Transistor type Solar Cell

We need to keep the photo charge collecting empty potential well always empty for a newly generated photo electron to be captured and swiftly be removed.



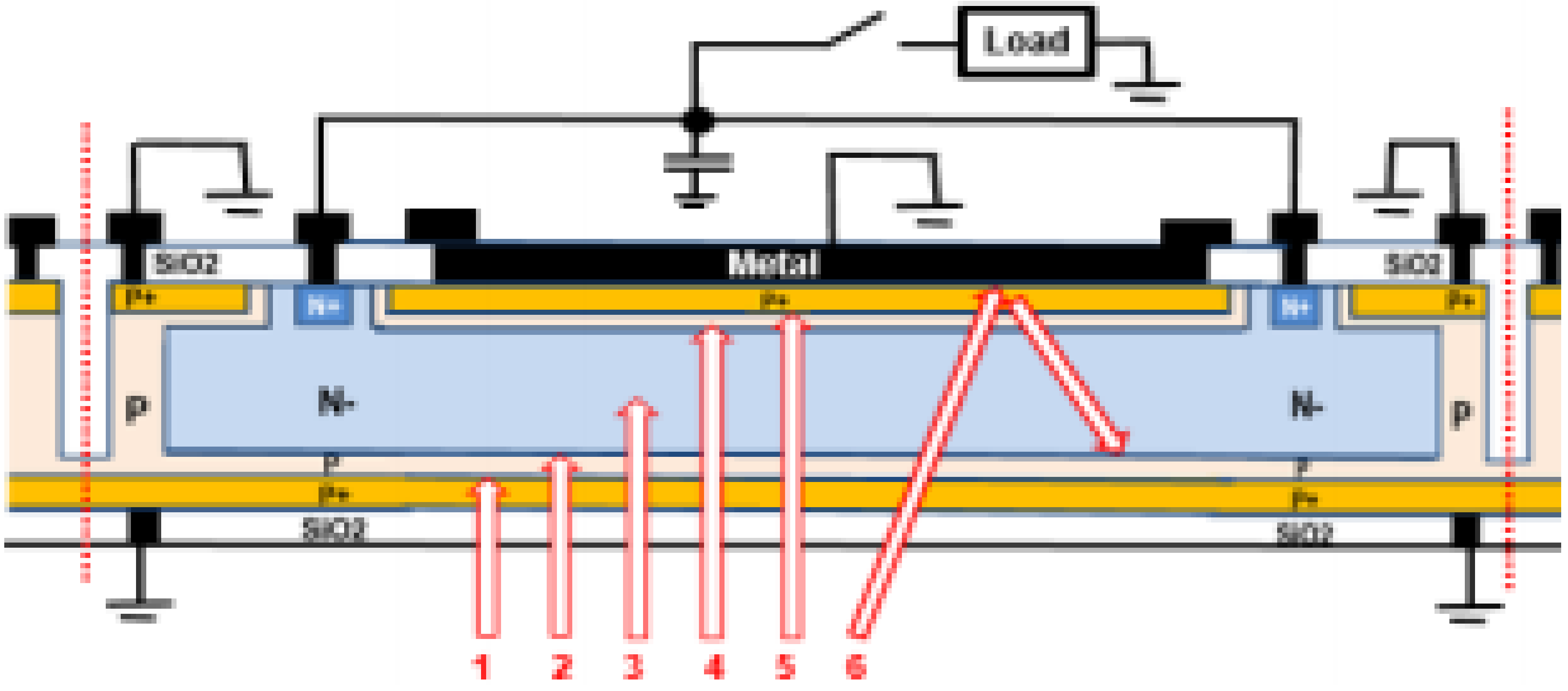
# 8 Double Junction Photo Transistor type Solar Cell

That is, the captured electron has to be removed immediately from the empty potential well to the adjacent charge collecting and storage N+ region.



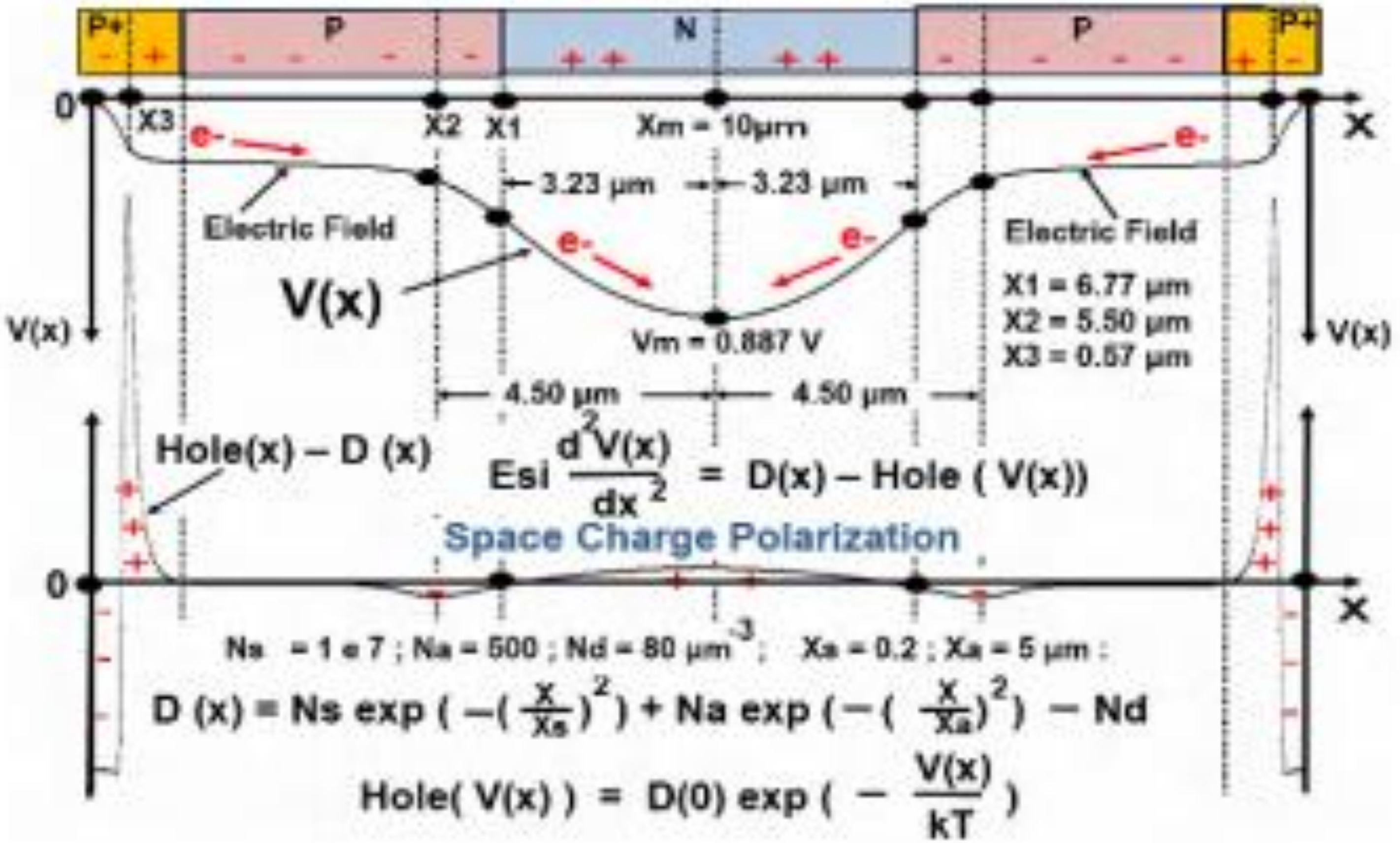
# 8 Double Junction Photo Transistor type Solar Cell

Another example of a symmetric P+PNPP+ junction type Pinned Photodiode (PPD) has two PN junction depletion region side by side, and also with the P+P barrier electric fields in both sides.



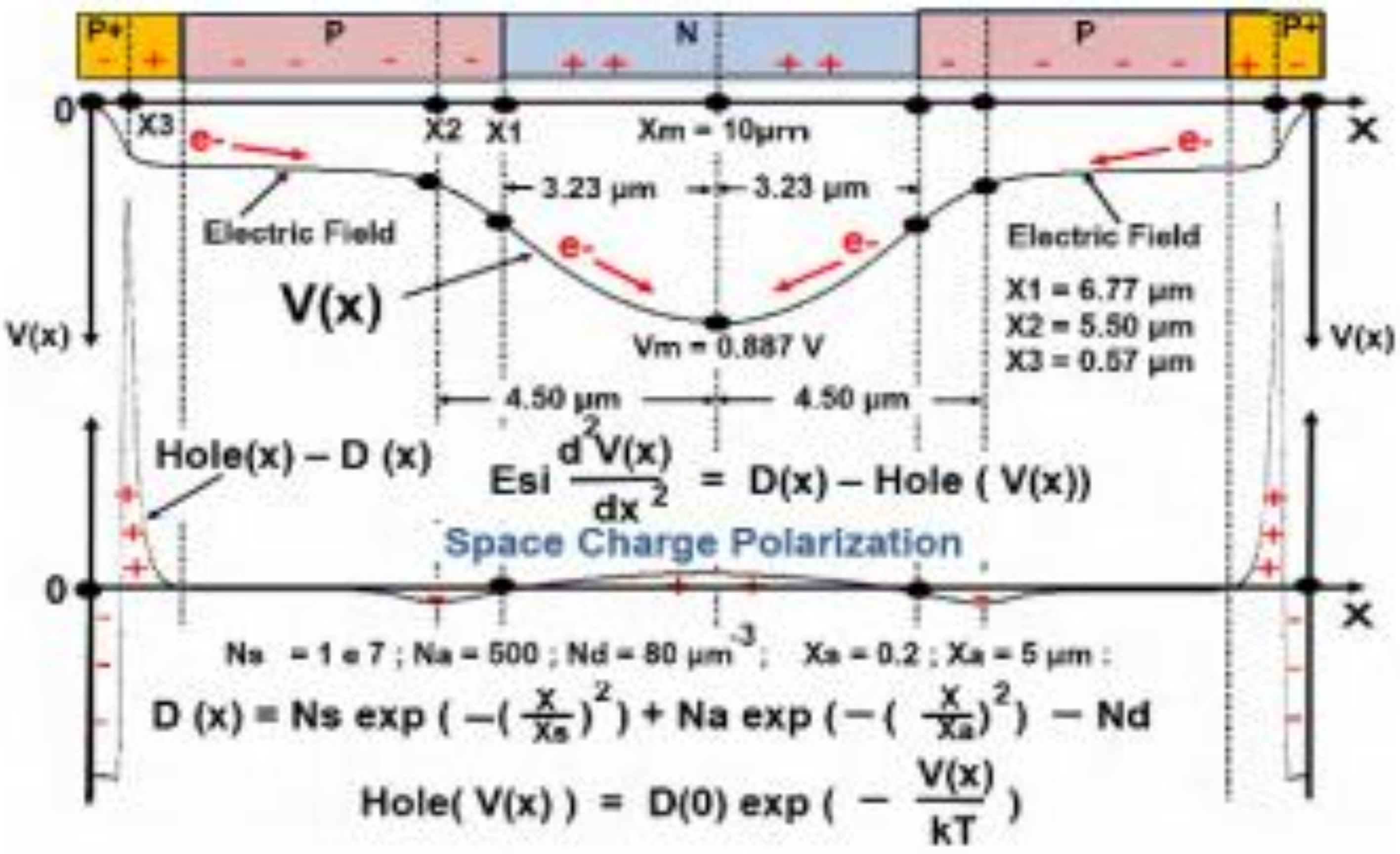
# 8 Double Junction Photo Transistor type Solar Cell

All of them contribute to quantum efficiency. The photoelectrons must be collected into the center lightly doped N region, but must be transferred quickly to the adjacent floating N+ heavily doped outlet.



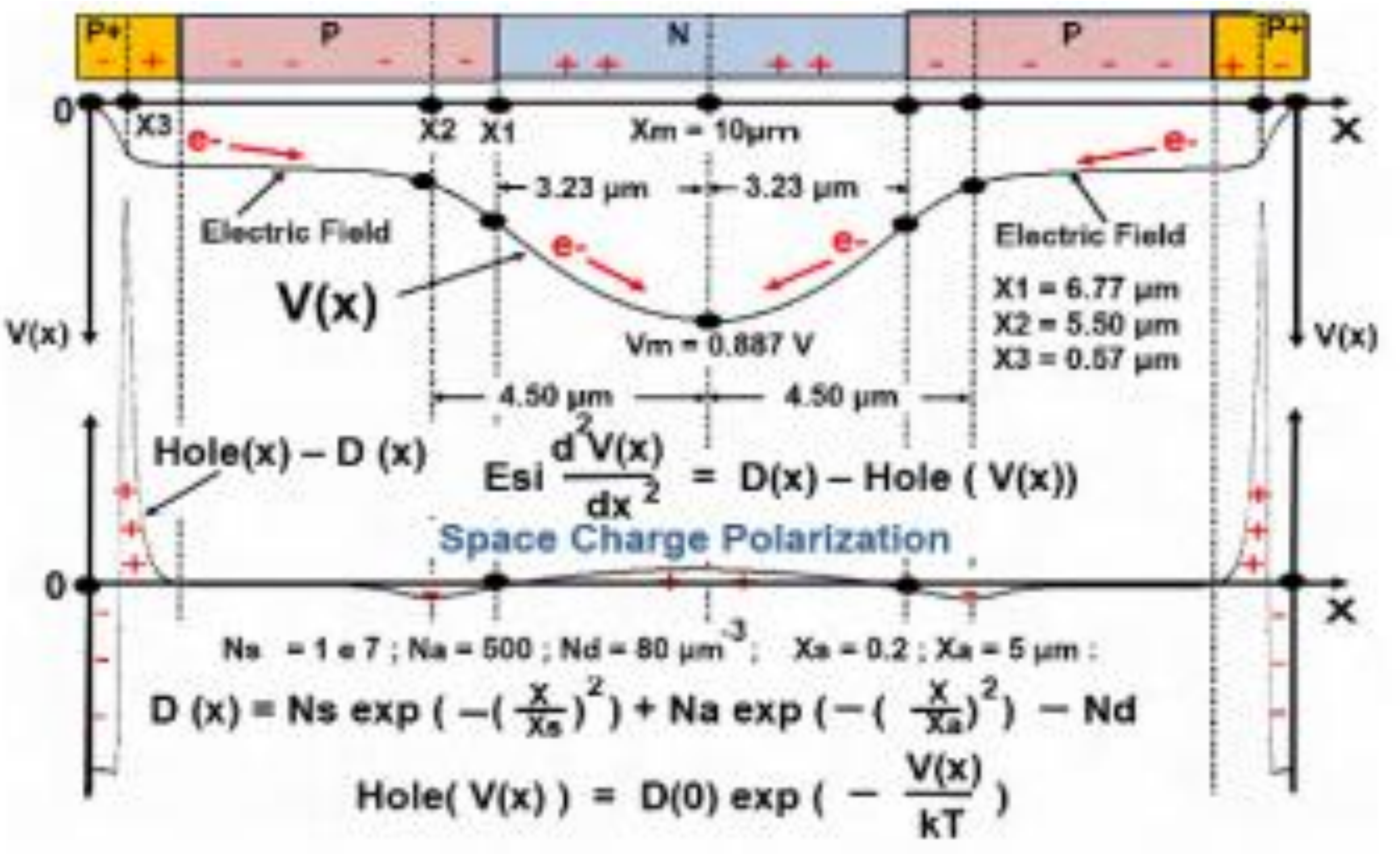
# 8 Double Junction Photo Transistor type Solar Cell

In this way, we can always keep the charge collecting N region always empty of electrons at the fixed or pinned empty potential, Vm.



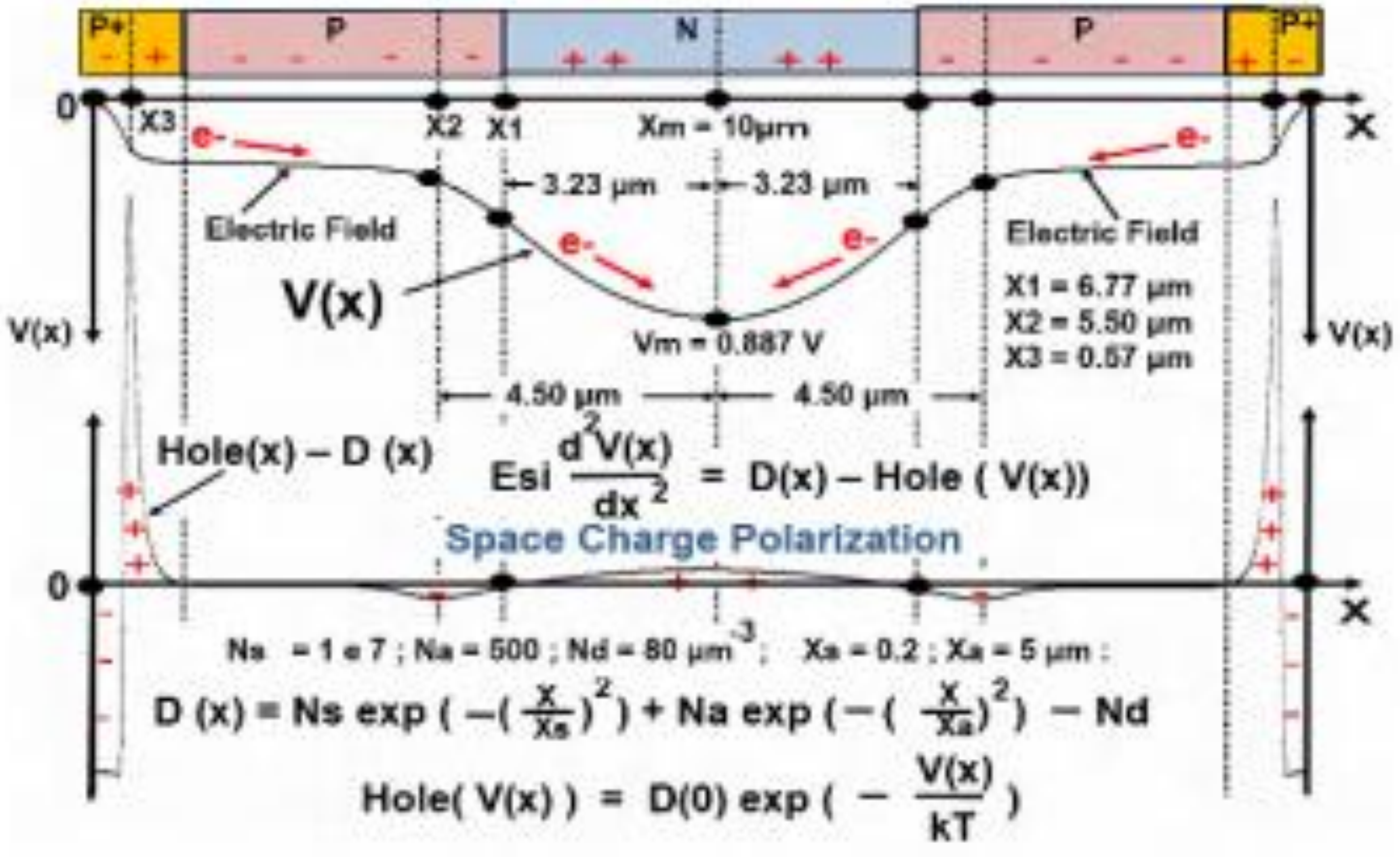
# 8 Double Junction Photo Transistor type Solar Cell

For this case study we have the surface P+ doping level Ns (NA+) of $1 \times 10^7$ e $\mu m^{-3}$ while P region doping level of 500 e $\mu m^{-3}$ and the pinned buried N region of 80 e $\mu m^{-3}$.



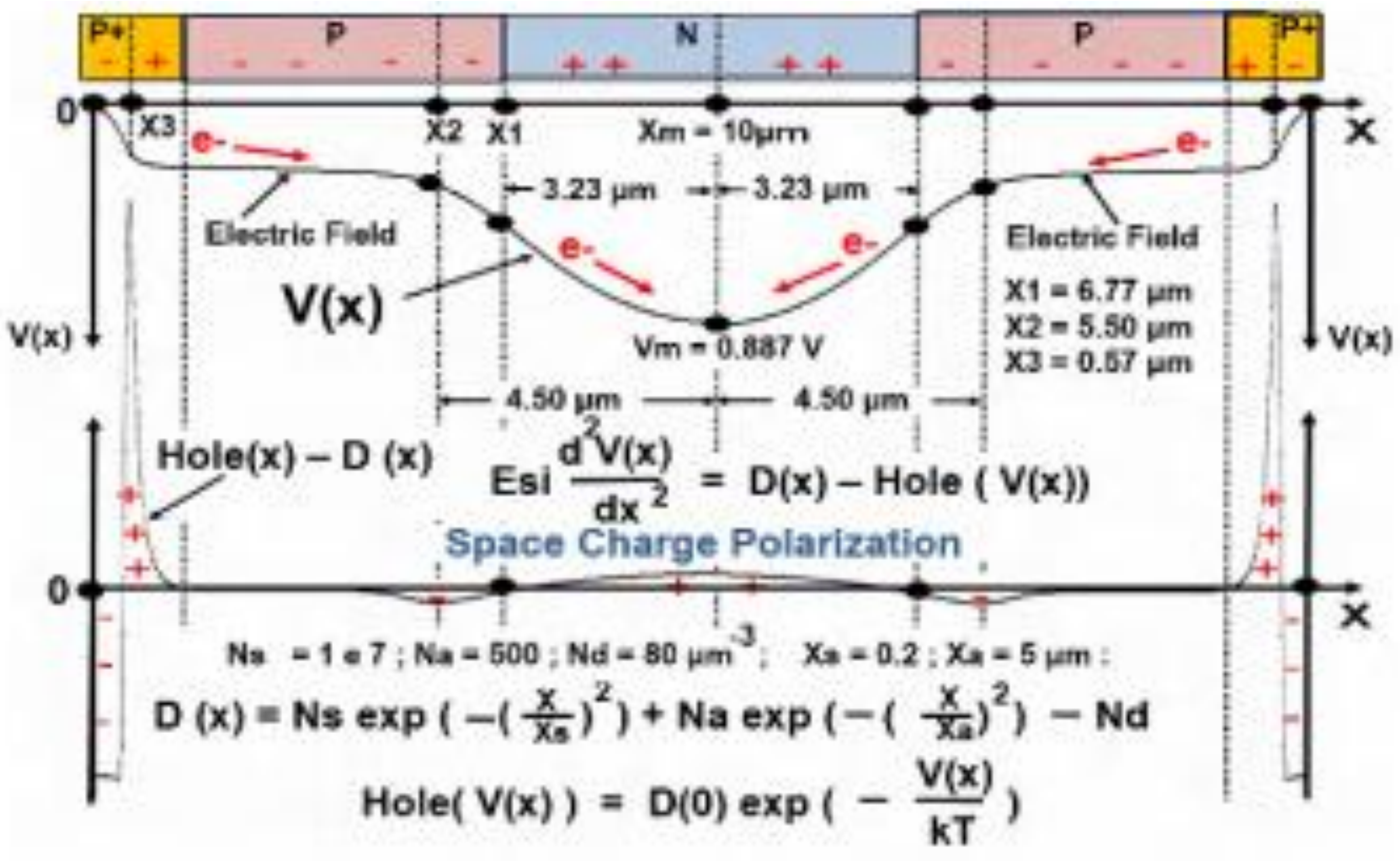
# 8 Double Junction Photo Transistor type Solar Cell

For this case study, having set the buried N region width to be 6.46 µm, the minimum potential Vm of 0.887 was obtained. This means that the solar cell output margin is expected to be Vout < $E_G$ –Vm = 1.100 – 0.887 volt = 0.223 volt.



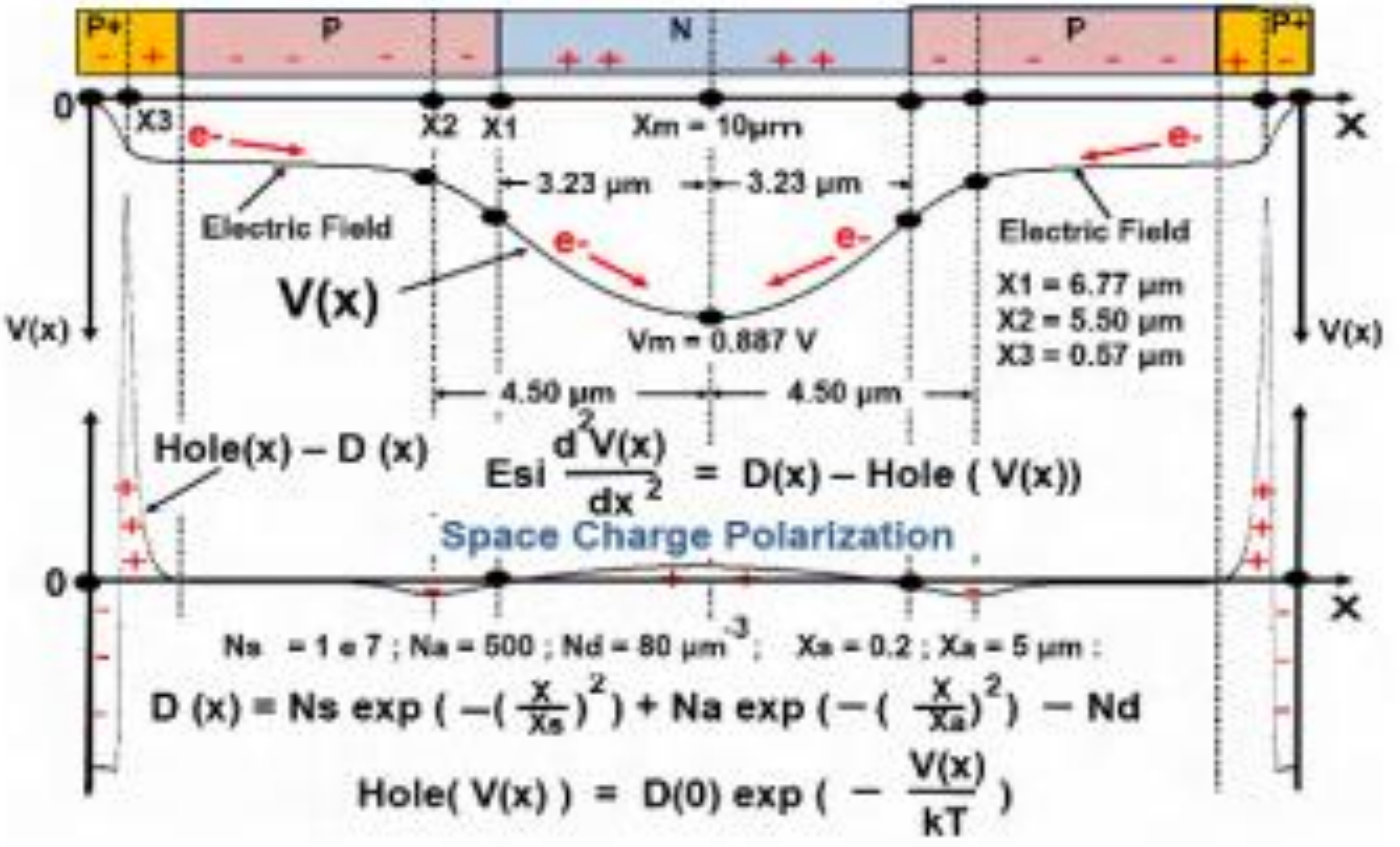
# 8 Double Junction Photo Transistor type Solar Cell

The ground level of the electron potential curve is set to be at the conduction band Ec of the P+ heavily doped surface accumulation region in this case.



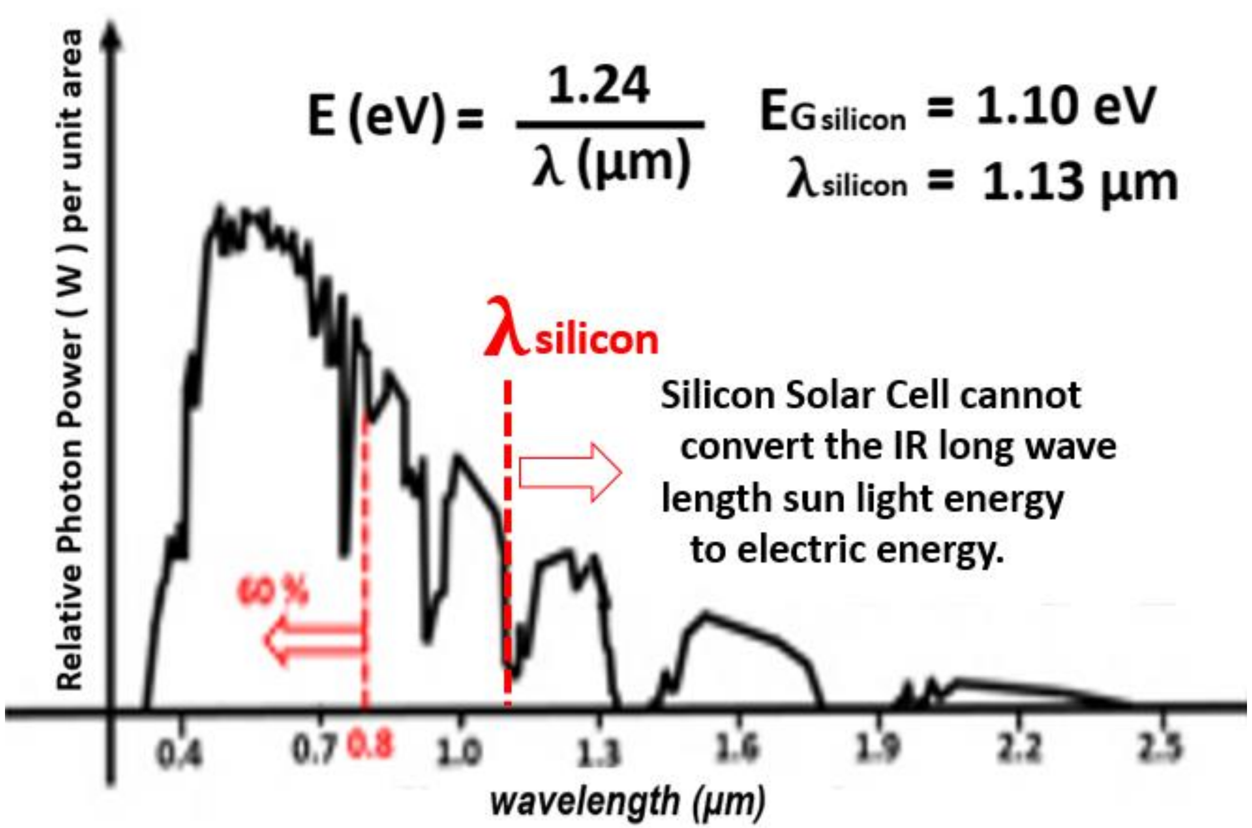
# 8 Double Junction Photo Transistor type Solar Cell

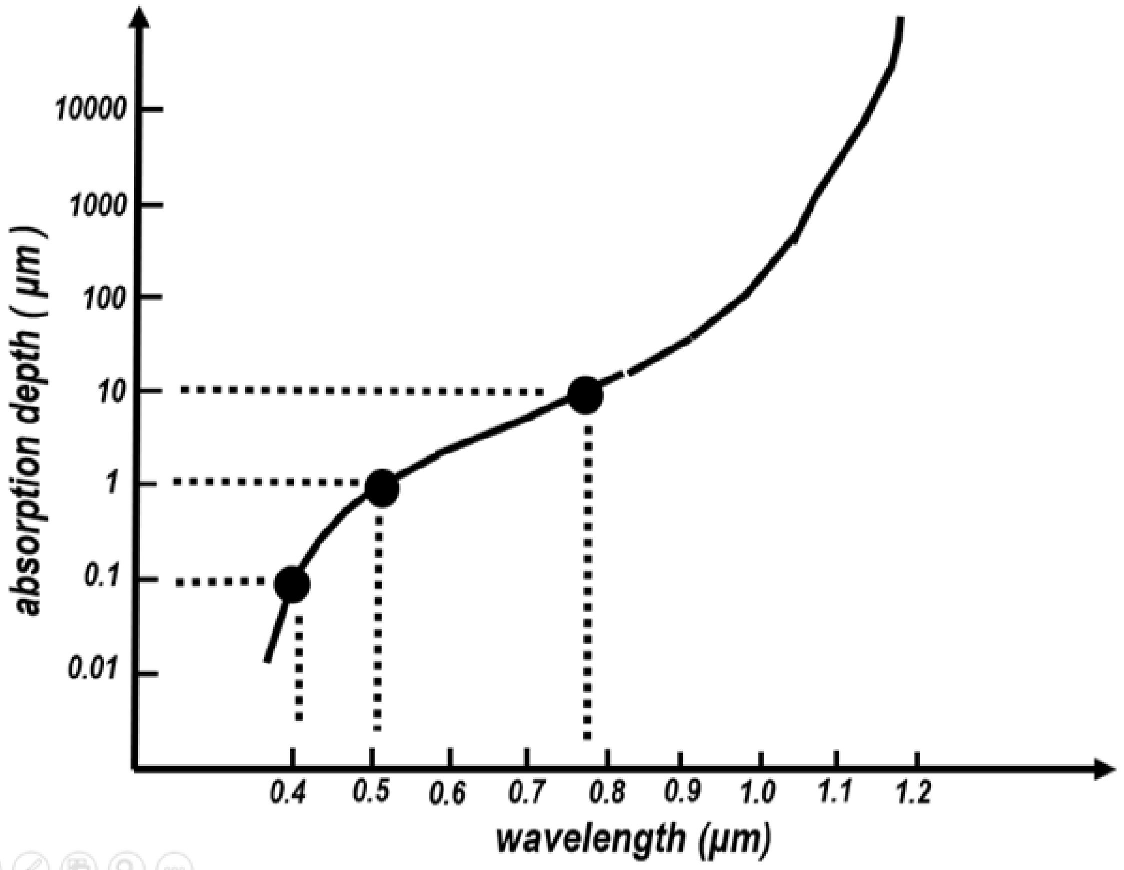
However, in this case study, the center depth of the buried N-region was designed to be 10 μm in depth in the silicon substrate.



## 8 Double Junction Photo Transistor type Solar Cell

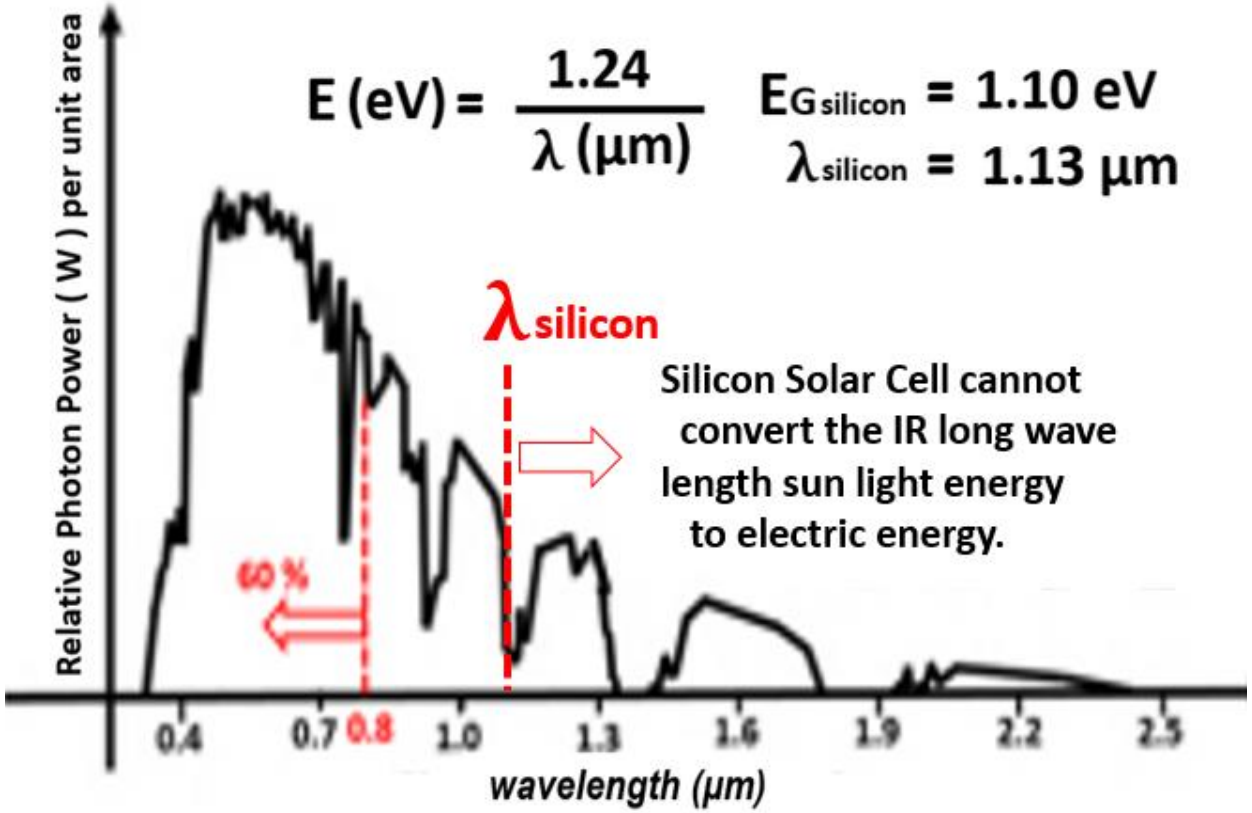
The visible light cannot reach the 10 μm depth in silicon. The light reaching the 10 μm depth in silicon is an IR light of a long wave length. In practical applications , IR filters are used.

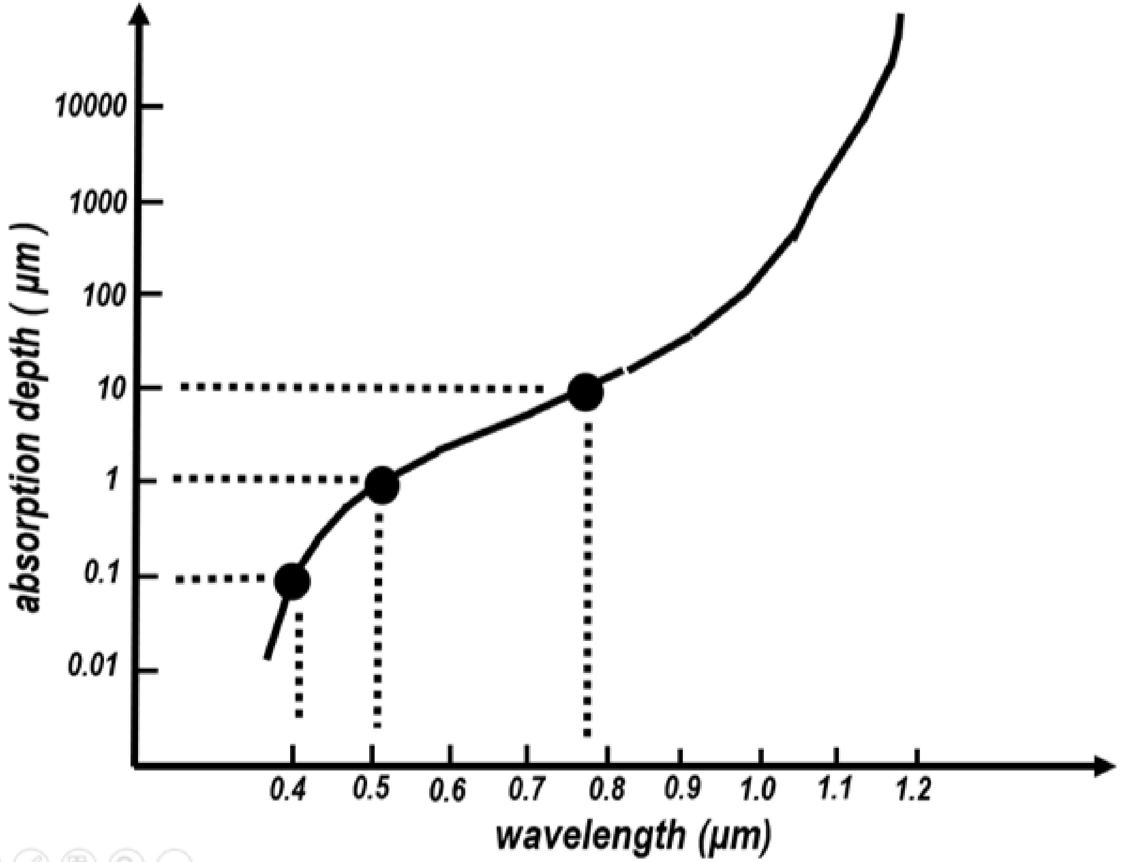


# 8 Double Junction Photo Transistor type Solar Cell

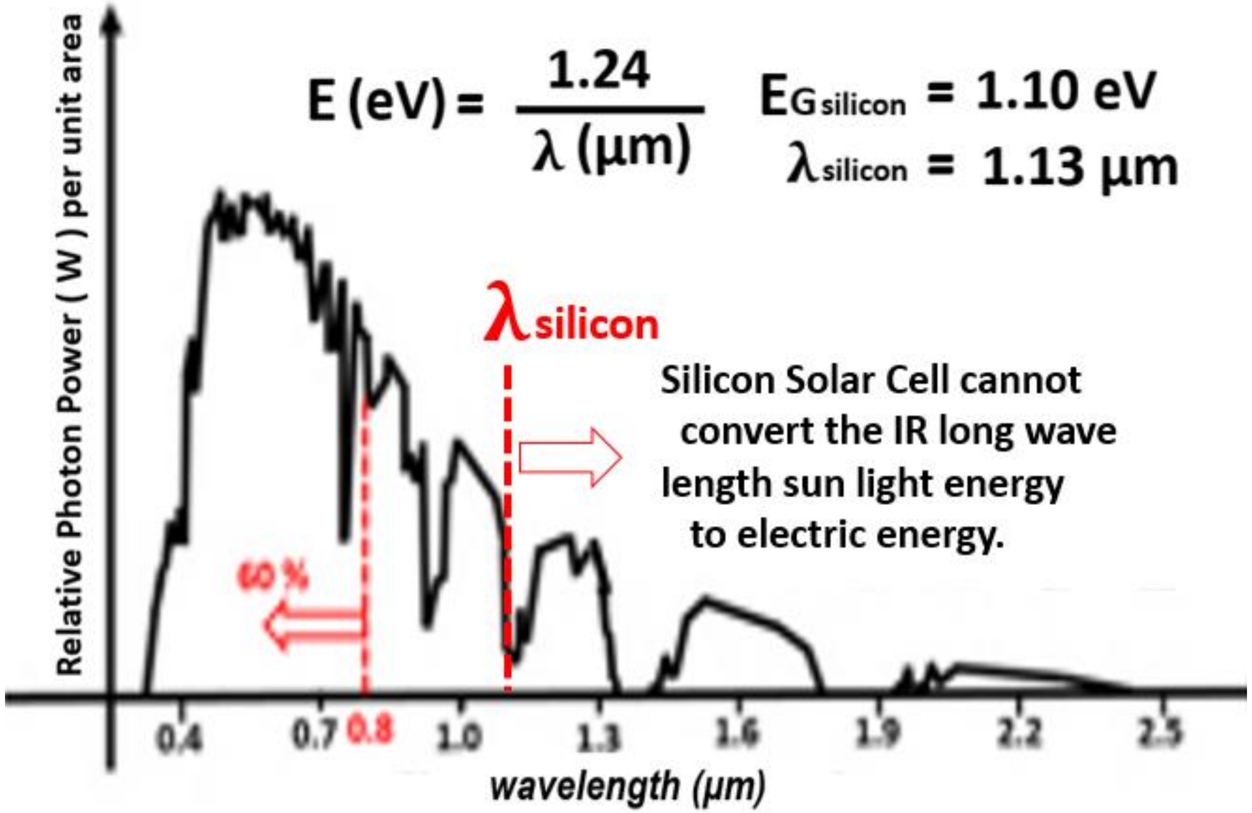
Even in solar cells, IR filters are attractive since they prevent from heating solar cell P/N by the sun light energy of the long wave length that cannot be converted to the electric energy.

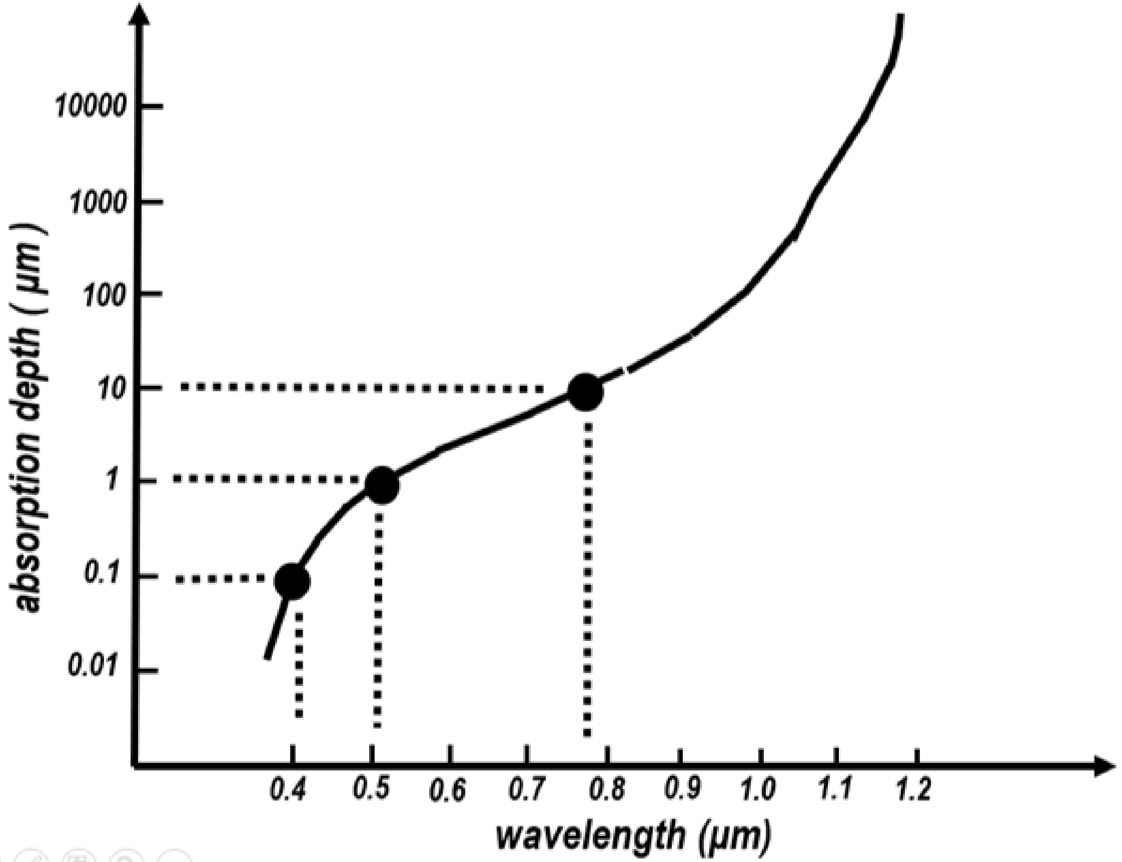


# 8 Double Junction Photo Transistor type Solar Cell

But IR filters themselves get hot. In solar cells, the sun light heating effect is a big issue. For 20 % efficient solar cells, 80 % sun light energy is lost into heat. If we can make 60% efficient solar cells, the heat issue may be lightened.



# 8 Double Junction Photo Transistor type Solar Cell

## Importance of Adjacent P+ Channel Stops in Pinned Photodiode

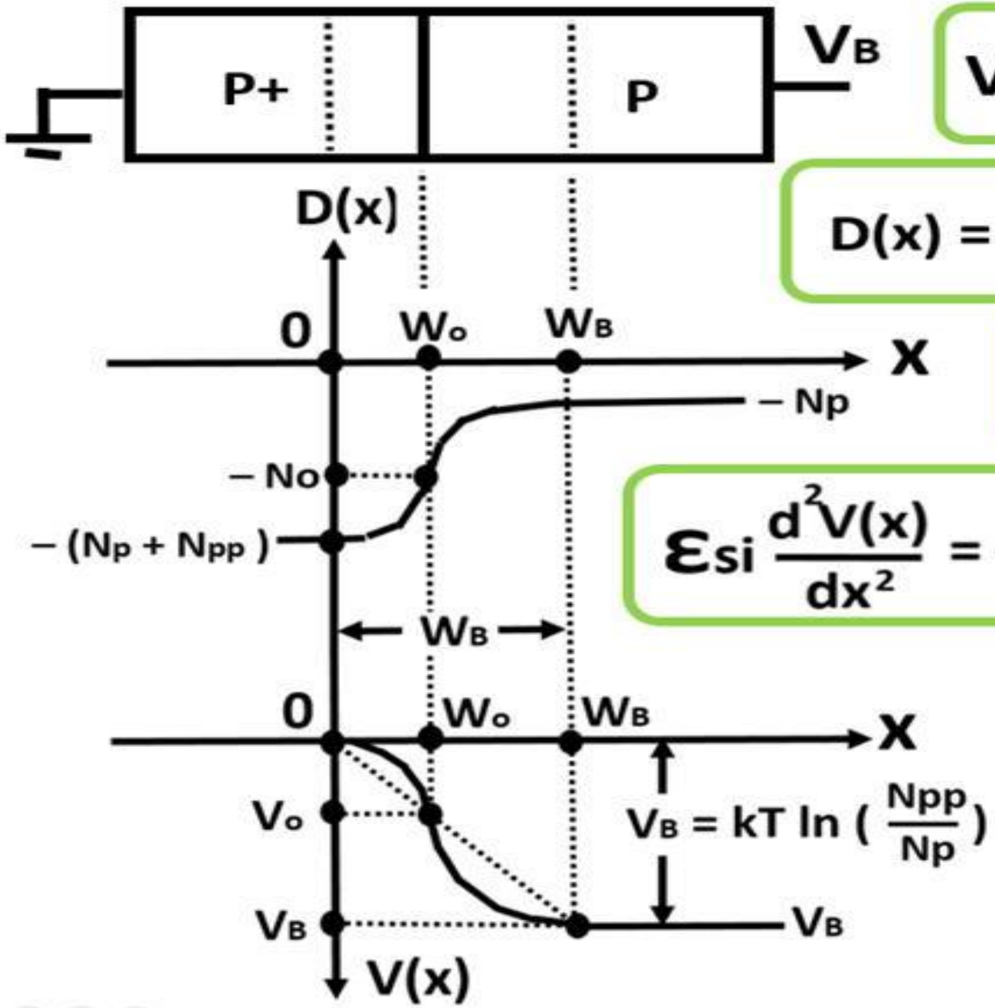
Hagiwara reported in his SSDM1978 paper the surface P+ ion implantation dosage of Qd = $2 \times 10^{13} cm^{-2}$. In order to have more than 95 % efficient surface photo electron and hole separations at the P+ Pinned surface, since the short wave blue light cannot penetrate into the silicon crystal more than 0.2 μm in depth, it is desired to have the surface Debye Length Lpp = $\sqrt{\varepsilon si\ kT/Npp}$ to be around 0. 01 μm. Set Qd = Lpp Npp. We have Npp = Qd / 0.01 μm = $2 \times 10^{19} cm^{-3}$ which is about the maximum degenerate silicon crystal impurity doping density. The surface P+ hole accumulation region must have this maximum degenerate hole carrier density, that has to be supplied at the P+ surface from the adjacent P+ channel stops. Pinned Photodiode must have an adjacent P+ channel stops region by necessity. Hagiwara reported in his SSDM1978 paper the P+NP junction type Pinned Photodiode with the adjacent P+ channel Stops in 1978.

# 8 Double Junction Photo Transistor type Solar Cell

The first Pinned Photodiode was proposed by Hagiwara in 1975 in his Japanese patent applications JPA 1975-127646, JPA 1975-127647 and 1975-134985. Then, the P+NP junction type Pinned Photodiode was applied in the 380H x 488 V Frame Transfer type CCD image sensor for the first time and reported in the SSDM1978 conference in Tokyo in 1978 . Subsequently, Hagiwara was invited at the CCD1979 conference in Edinburgh, Scotland UK in 1979, and then in the ECS1980 conference in St. Luis , USA in 1980, for this P+NP junction type Pinned Photodiode Image Sensor works. The short wave blue light cannot penetrate more than 0.1 μm into the silicon crystal in depth. The surface barrier potential VB of the Pinned P+P surface P+PNPP+ double junction type Pinned Photodiode is now applied to realize a very high quantum efficiency solar cell of more than 60 % expectedly. The surface barrier width WB for the photo electron and hole pairs separation was found to be more than four times of the estimated P+P Debye width by a simple calculation.

# 8 Double Junction Photo Transistor type Solar Cell

## The Barrier Potential $V_B$ and the Width $W_B$




$$V_B = kT \ln \left( \frac{N_{pp}}{N_p} \right)$$

$$W_B = W_o \frac{V_B}{V_o}$$

$$D(x) = -N_p - N_{pp} \exp\left( -\frac{x^2}{R^2} \right) \quad \text{for } x > 0$$

$$\frac{d^2 D(x)}{dx^2} = 0 \quad \text{at } x = W_o$$

$$W_o = \frac{R}{\sqrt{2}}$$

$$\varepsilon_{si} \frac{d^2 V(x)}{dx^2} = -D(x) - (N_p + N_{pp}) \exp\left( -\frac{V(x)}{kT} \right)$$

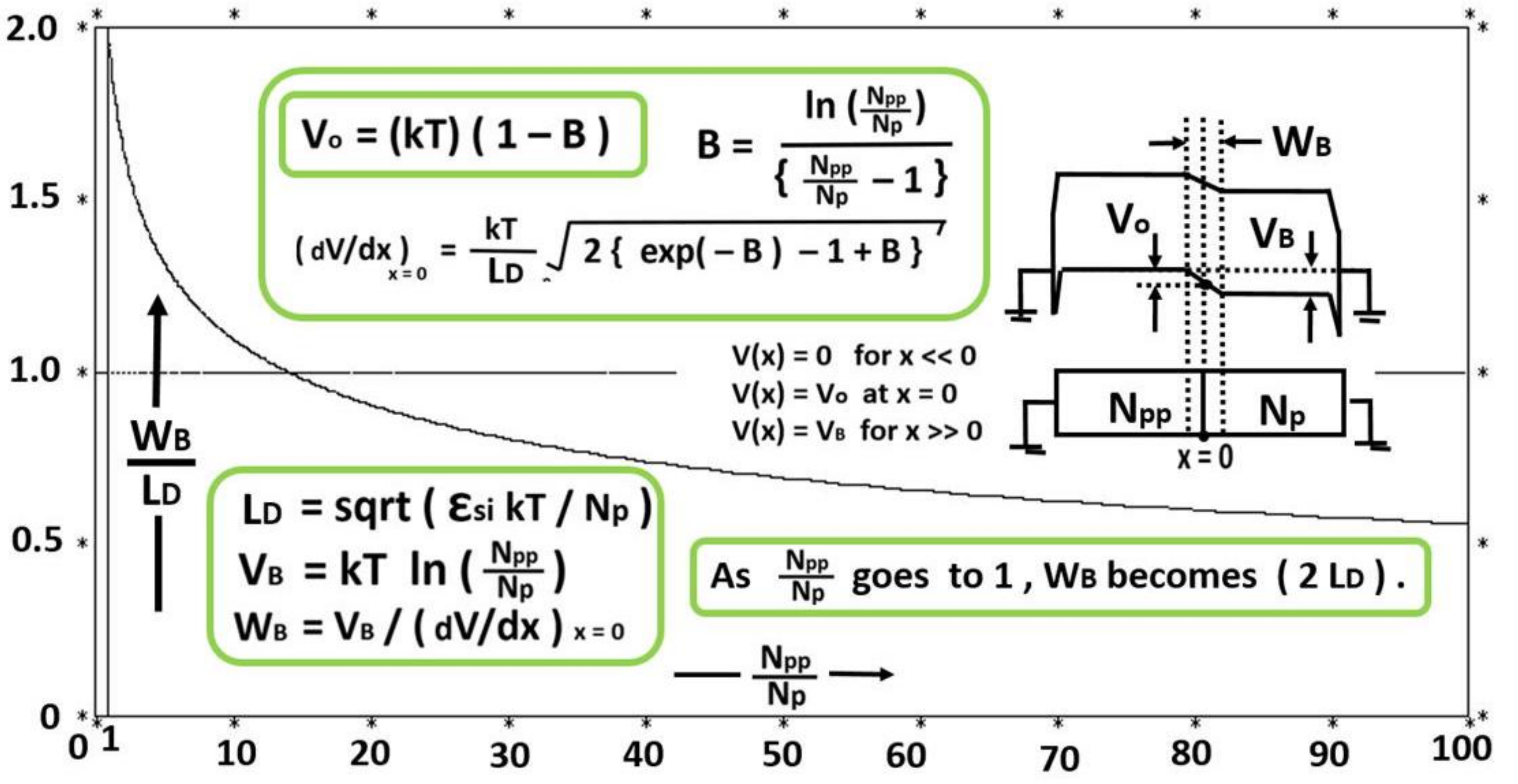
$$V(x) = 0 \quad \text{at } x = 0$$

$$V(x) = V_B \quad \text{at } x = W_B$$

$$N_o = N_p + N_{pp} \exp\left( -\frac{W_o^2}{R^2} \right)$$

$$N_o = (N_p + N_{pp}) \exp\left( -\frac{V_o}{kT} \right)$$

# 8　Double Junction Photo Transistor type Solar Cell




**Barrier Height VB and Barrier Width WB for the P+P abrupt doping profile**

# 8 Double Junction Photo Transistor type Solar Cell

**P+P Gaussian Doping Profile**

$D(x) = -Np - Npp \exp(-x^2/R^2)$

$Np = 10000$ e/μm$^3$

$Npp = 100000$ e/μm$^3$

$R = 0.10$ μm

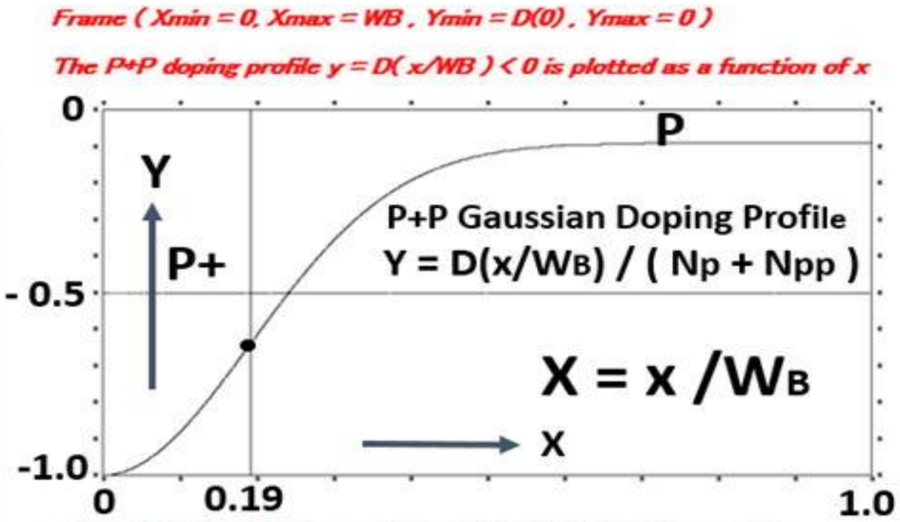
$Wo = R / \text{sqrt}(2.0) = 0.070711$ μm

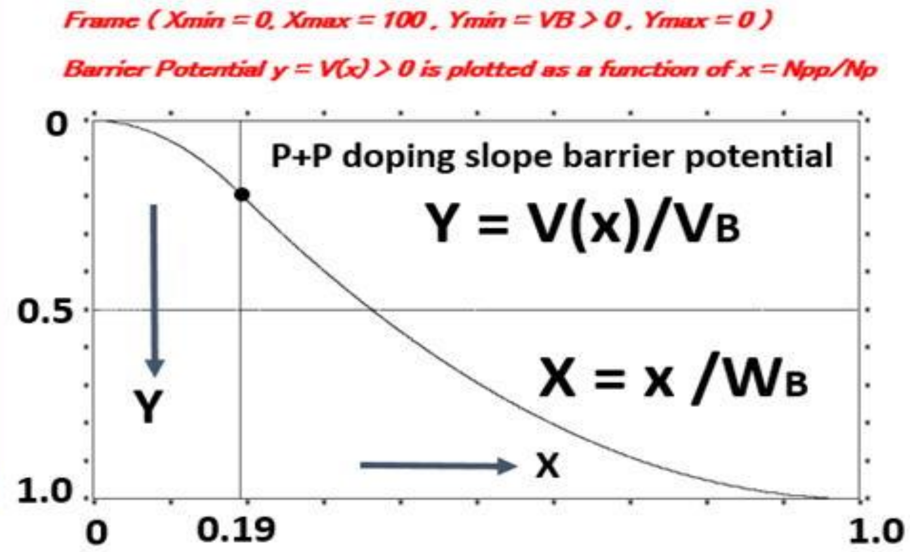
$No = Np + Npp*\exp(-0.5)$
$= 70653.065971$ e/μm$^3$

$Vo = kT*\log((Np + Npp)/No)$
$= 0.011466$ volt

$VB = kT*\log(Npp/Np) = 0.059637$ volt

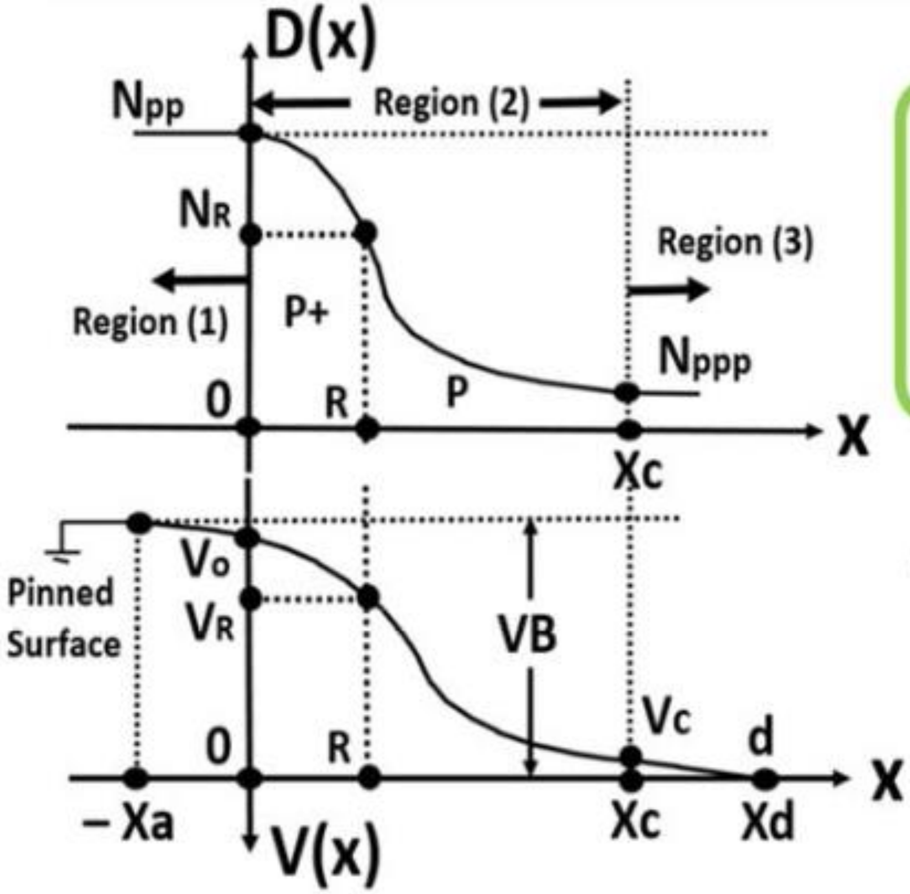
$WB = Wo*VB/Vo = 0.367784$ μm
$WB/Wo = VB/Vo = 5.201245$
$Wo/WB = Vo/VB = 0.192262$



# 8 Double Junction Photo Transistor type Solar Cell

**Solve Poisson's Equation for the barrier potential V(x) of the P+P Pinned Surface Gaussian Doping Profile D(x).**




Gaussian Doping Profile D(x).

(1) For $x < 0$, $D(x) = D(0) = N_{pp}$ ;

(2) For $0 < x < X_c$,

$D(x) = N_p + (N_{pp} - N_p) \exp(-x^2/R^2)$ ;

(3) For $X_c < x$, $D(x) = D(X_c) = N_{ppp}$ ;

**Poisson's Equation**

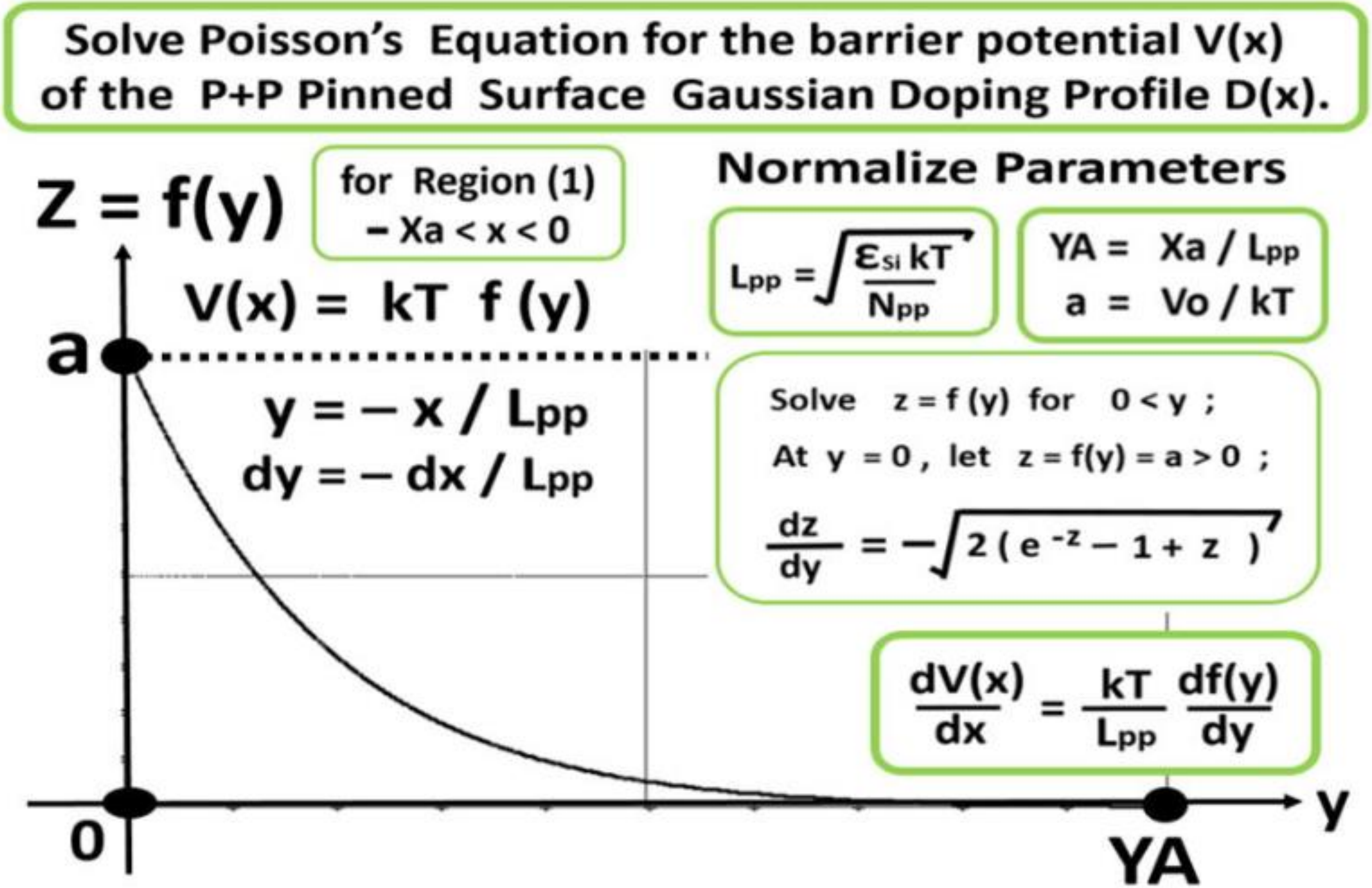
$$\varepsilon_{Si} \frac{d^2V(x)}{dx^2} = D(x) - N_{pp} \exp(-V(x)/kT)$$

At $x = -\infty$, $V(x) = 0$ ;

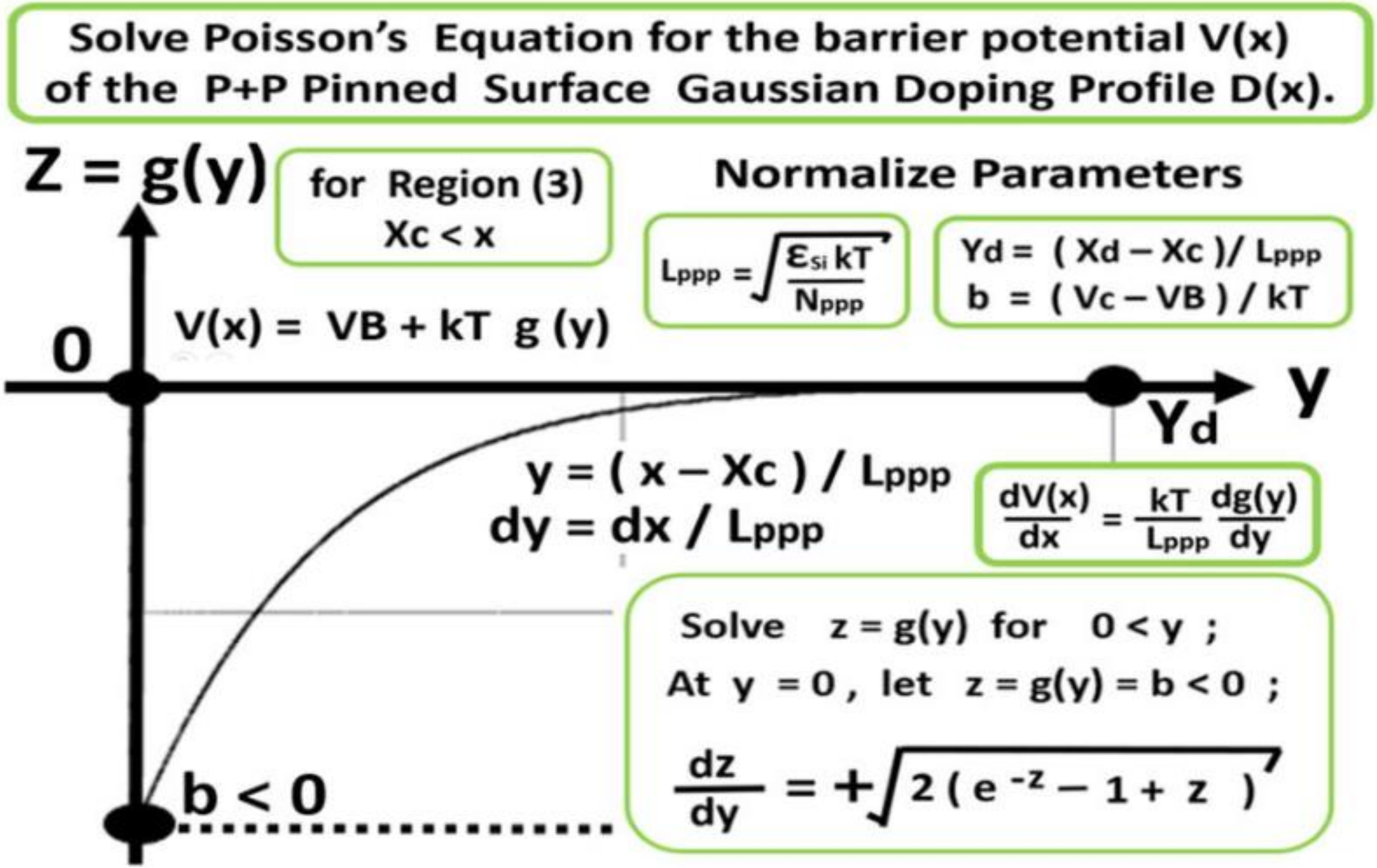
At $x = +\infty$, $V(x) = VB$ ;

$VB = kT \ln(N_{pp}/N_{ppp})$ ;

# 8 Double Junction Photo Transistor type Solar Cell



# 8 Double Junction Photo Transistor type Solar Cell



# 8 Double Junction Photo Transistor type Solar Cell

**Solve Poisson's Equation for the barrier potential V(x) of the P+P Pinned Surface Gaussian Doping Profile D(x).**

for Region (2) $0 < X < X_c$ solve Poisson Equation by iteration.

- Step (1) Let V[0] = Vo ( any value first )
- Step (2) Get V[1] = V[0] + dx * (dV/dx)
- Step (3) For i = 2 to i = N, from V[i-1] and V[i-2] obtain V[i] by the Poisson's equation
- Step (4) Get V[N-1] and Vc = V[N] .
- Step (5) Get dV(x)/dy = ( V[N] – V[N-1] )/dx
- Step (6) Let z = ( Vc – VB )/ kT and obtain dg(y)/dy
- Step (7) Check Lppp * dV(x)/dx = kT * dg(y)/dy .
- Step (8) If not, go back to Step(1) for another Vo.

At $x = 0$, $z = V_o / kT$

$$\frac{dV(x)}{dx} = \frac{kT}{L_{pp}} \frac{df(y)}{dy}$$

$$\frac{df(y)}{dy} = -\sqrt{2\left(e^{-z} - 1 + z\right)}$$

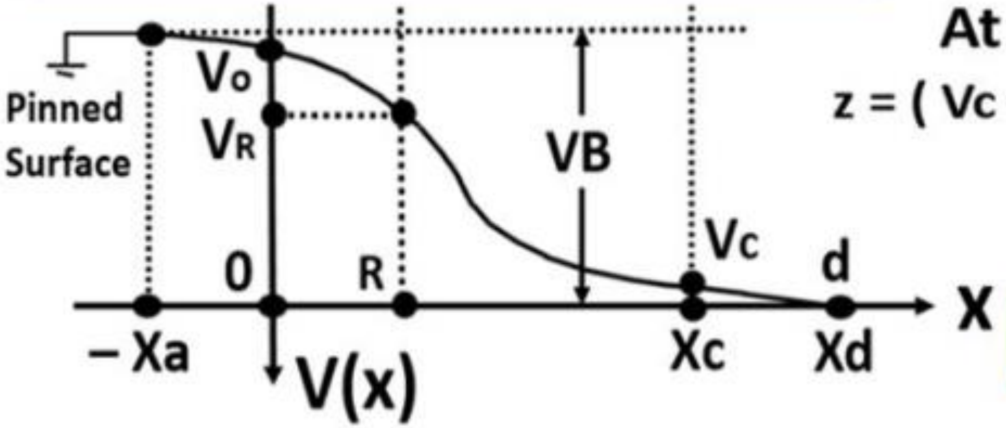
Poisson's Equation

$$\varepsilon_{Si} \frac{d^2V(x)}{dx^2} = D(x) - N_{pp} \exp\left(-V(x)/kT\right)$$

At $x = X_c$, $z = (V_c - V_B)/kT$

$$\frac{dV(x)}{dx} = \frac{kT}{L_{ppp}} \frac{dg(y)}{dy}$$

$$\frac{dg(y)}{dy} = +\sqrt{2\left(e^{-z} - 1 + z\right)}$$




$$VBB = V[N] - kT * Z$$

# 8 Double Junction Photo Transistor type Solar Cell

kT = 0.0259 eV , Esi = 648 e/volt • um

R = 0.100000 um , Xc = 1.000000 um

N =40000 dx = Xc/N = 0.000025 um

Np =100, Npp = 1000, Nppp = 100.000000

Lp = 0.409673 Lpp = 0.129550 Lppp =0.409673

VB =1000* kT * log( Npp/Nppp ) = 59.636954

Nr =D(x) = 431.091497 at x = R = 0.100000

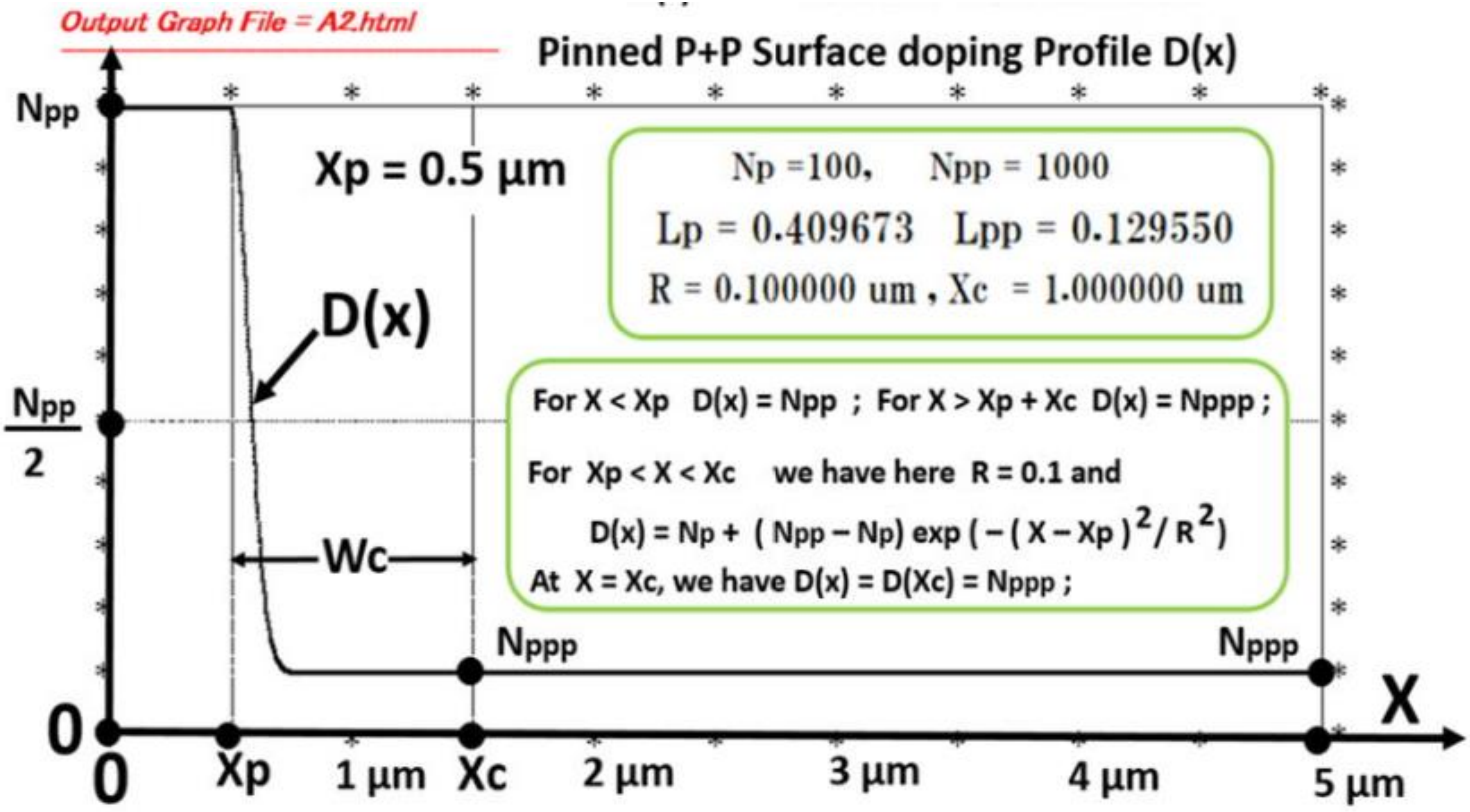
For Vo = 0.0106401053200 ~ 0.0164201053193,
we obtained
Vc = 0.056133035 and
VB = 0.059636954
with Err ~ 0.00000.

We set now
Vo = 0.010642010531965
for later computations.

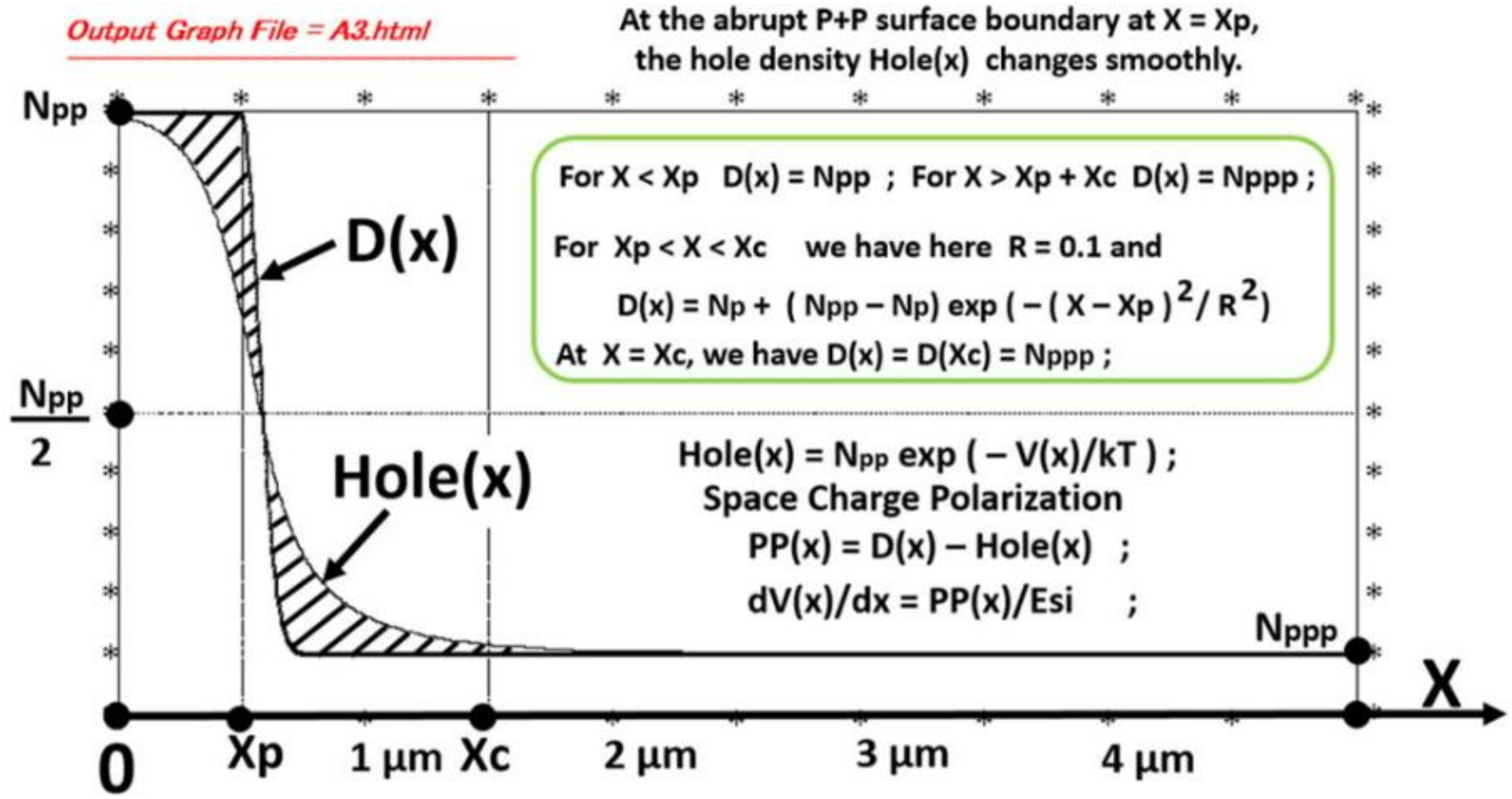
```
dvdxN= Lppp*( VV[N] - VV[N-1] )/dx;
z = ( Vc - VB ) / kT;
dgdy = kT*sqrt ( 2 * ( exp( - z ) - 1 + z ) );
Err = ( dvdxN - dgdy )*100000 ;
```

```
Command Prompt - a

100000000000000*VVA = 1064201053192.000000

100000000000000*VVB = 1064201053201.000122

Vo = 1064201.053201   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000001
Vo = 1064201.053200   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053199   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053198   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053197   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053197   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053196   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053195   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
Vo = 1064201.053194   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = -0.000000
Vo = 1064201.053193   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = -0.000000
Vo = 1064201.053192   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = -0.000001

100000000000000*Vo = 1064201053196.500000

Vo = 1064201.053197   Vc[40001] = 56.133035   Lppp*( v -vv )/dx = 0.003585   kT*dgdy = 0.003585   Err = 0.000000
```

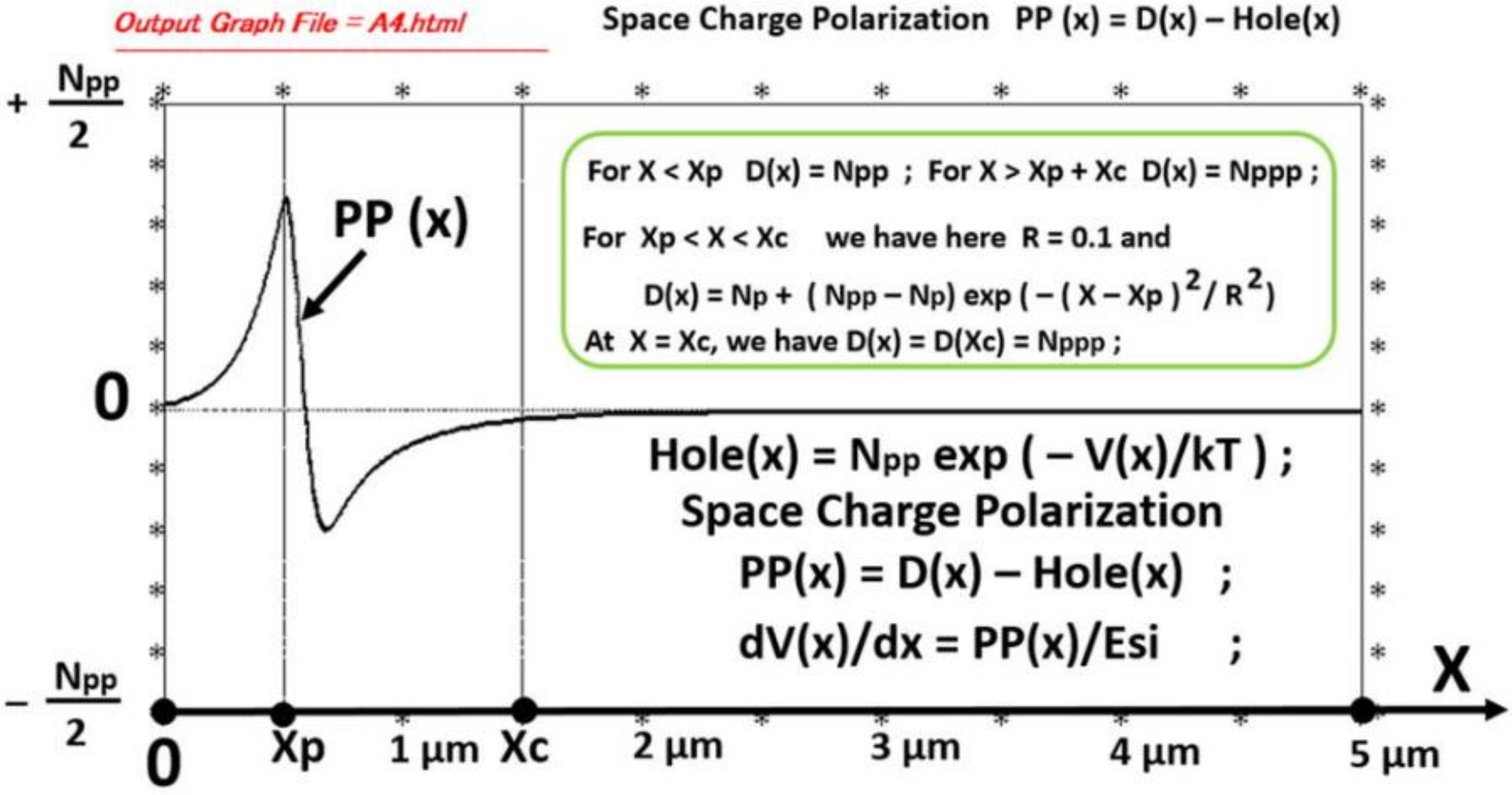
# 8 Double Junction Photo Transistor type Solar Cell



# 8 Double Junction Photo Transistor type Solar Cell



# 8 Double Junction Photo Transistor type Solar Cell



# 8 Double Junction Photo Transistor type Solar Cell

Photo Electron and Hole Pairs Separation at the P+P Pinned Surface Barrier Potential (VB) in a very high quantum efficiency P+PNPP+ junction Pinned Photo Diode Solar Cell proposed and applied for a patent ( JPA 2020-131313 ) by Yoshiaki Hagiwara.

**Numerical Calculation Model of the P+P Surface Pinned Photodiode Solar Cell**

Very Effective Photo Electron and Hole Pairs Separation in the P+P Pinned Surface Barrier Potential VB

$$VB = kT \ln\left(\frac{Npp}{Np}\right)$$

Region (1) for $X < 0$

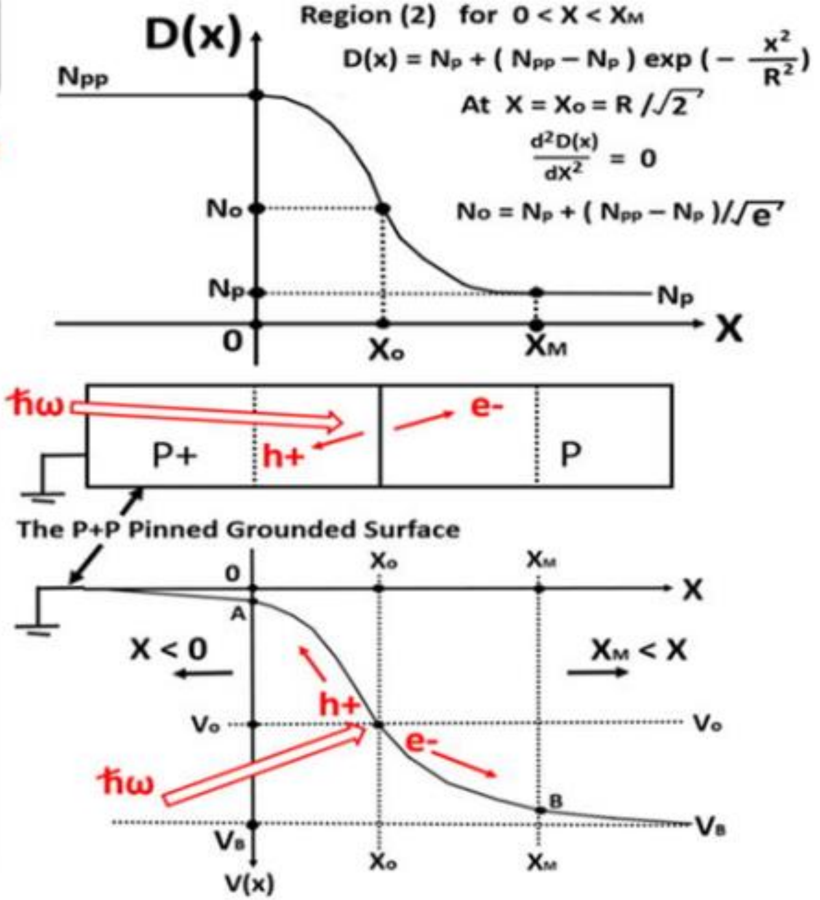
$$\varepsilon_{Si} \frac{d^2V(x)}{dX^2} = N_{pp}\left\{ 1 - \exp\left( - \frac{V(x)}{kT} \right)\right\}$$

Region (2) for $0 < X < X_M$

$$\varepsilon_{Si} \frac{d^2V(x)}{dX^2} = D(x) - N_{pp} \exp\left( - \frac{V(x)}{kT} \right)$$

Region (3) for $X_M < X$

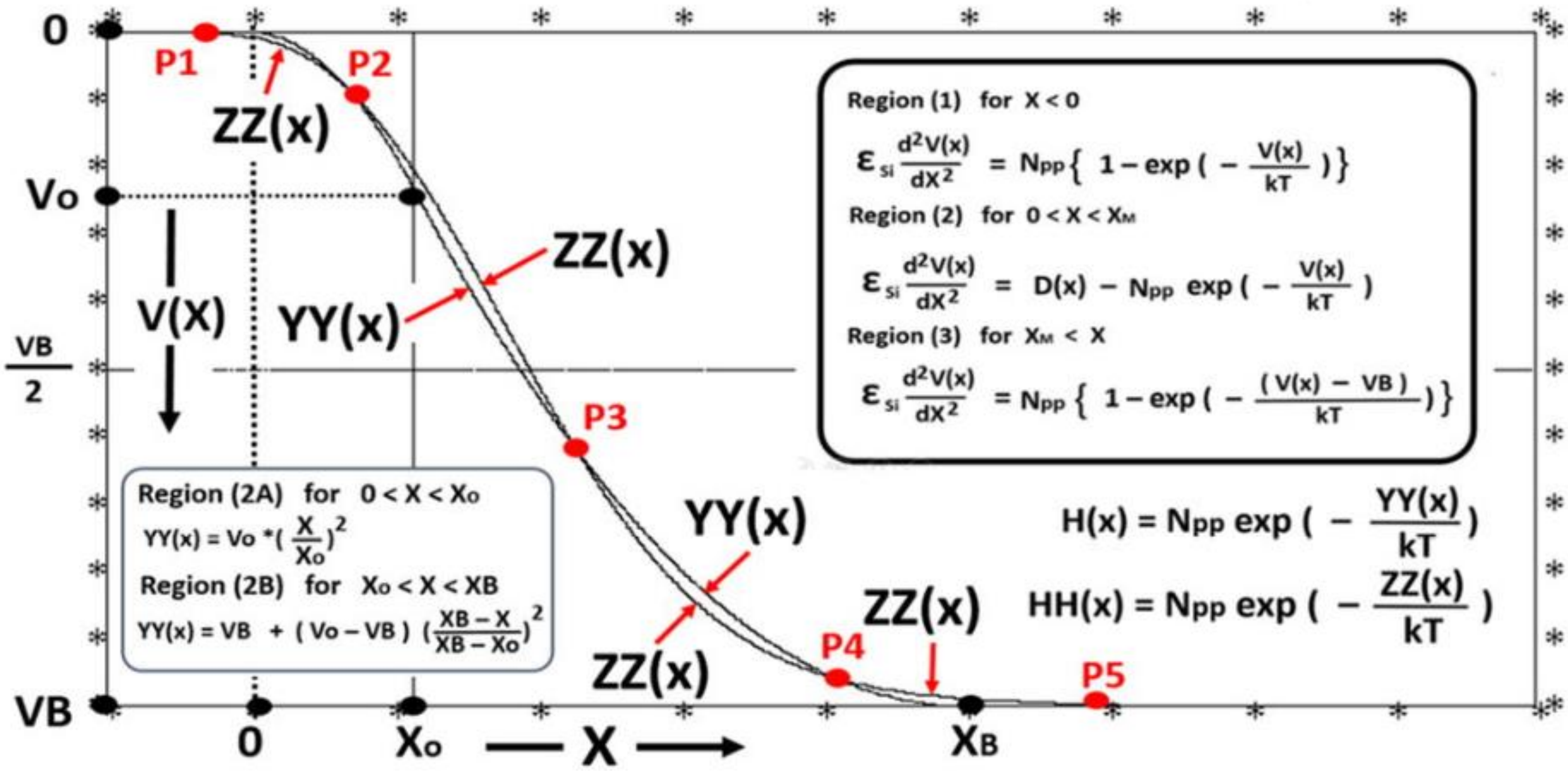
$$\varepsilon_{Si} \frac{d^2V(x)}{dX^2} = N_{pp}\left\{ 1 - \exp\left( - \frac{(V(x) - VB)}{kT} \right)\right\}$$



# 8 Double Junction Photo Transistor type Solar Cell

Photo Electron and Hole Pairs Separation at the P+P Pinned Surface Barrier Potential (VB) in a very high quantum efficiency P+PNPP+ junction Pinned Photo Diode Solar Cell proposed and applied for a patent ( JPA 2020-131313 ) by Yoshiaki Hagiwara.

*Exact Numerical Barrier Potential ZZ(x) and Initial Value YY(x) are compared* Output = A1.html




Region (1) for $X < 0$

$$\varepsilon_{Si} \frac{d^2V(x)}{dX^2} = N_{PP} \left\{ 1 - \exp\left( - \frac{V(x)}{kT} \right) \right\}$$

Region (2) for $0 < X < X_M$

$$\varepsilon_{Si} \frac{d^2V(x)}{dX^2} = D(x) - N_{PP} \exp\left( - \frac{V(x)}{kT} \right)$$

Region (3) for $X_M < X$

$$\varepsilon_{Si} \frac{d^2V(x)}{dX^2} = N_{PP} \left\{ 1 - \exp\left( - \frac{(V(x) - VB)}{kT} \right) \right\}$$

Region (2A) for $0 < X < X_o$

$$YY(x) = V_o * \left( \frac{X}{X_o} \right)^2$$

Region (2B) for $X_o < X < XB$

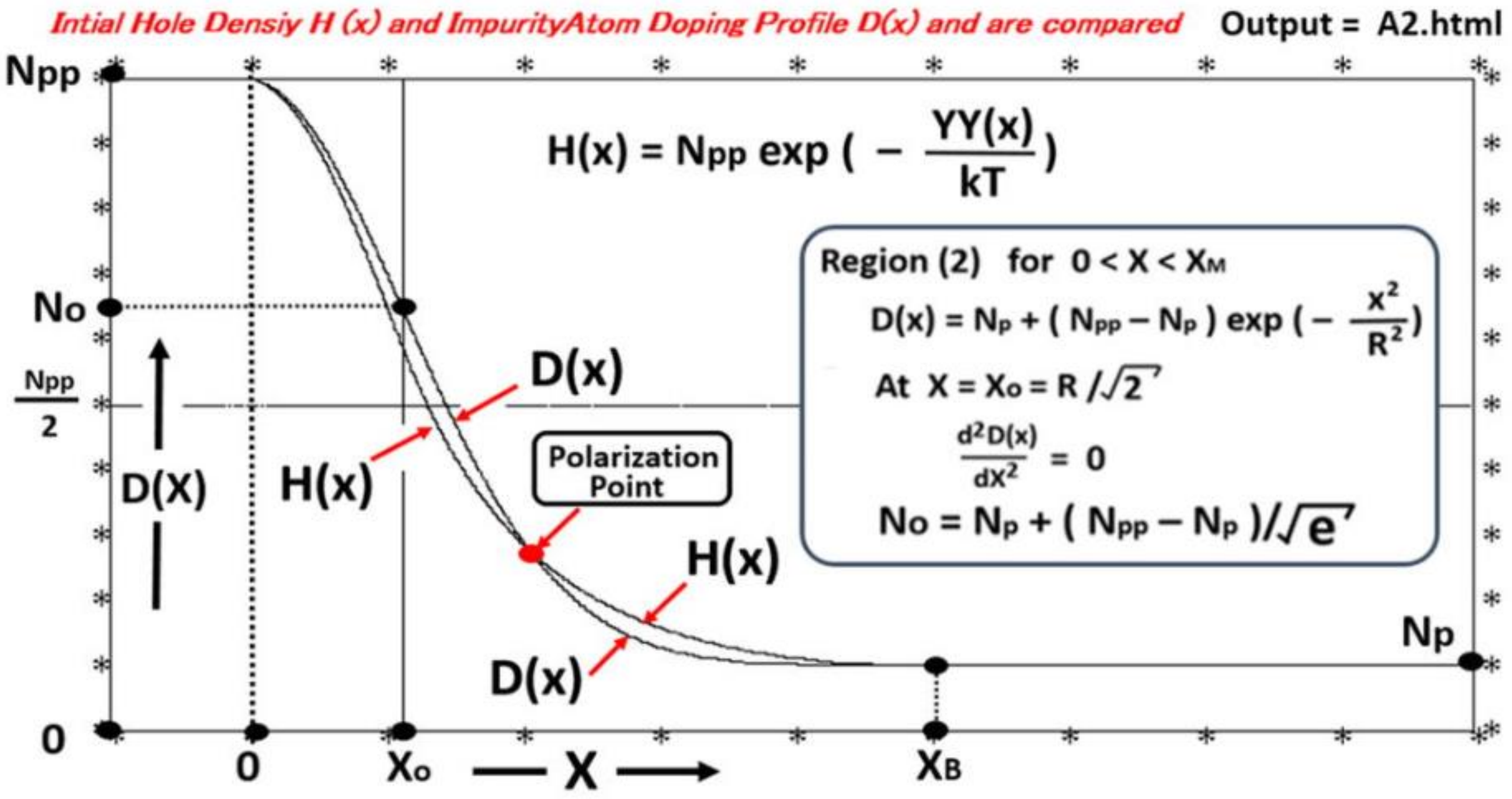
$$YY(x) = VB + (V_o - VB) \left( \frac{XB - X}{XB - X_o} \right)^2$$

$$H(x) = N_{PP} \exp\left( - \frac{YY(x)}{kT} \right)$$

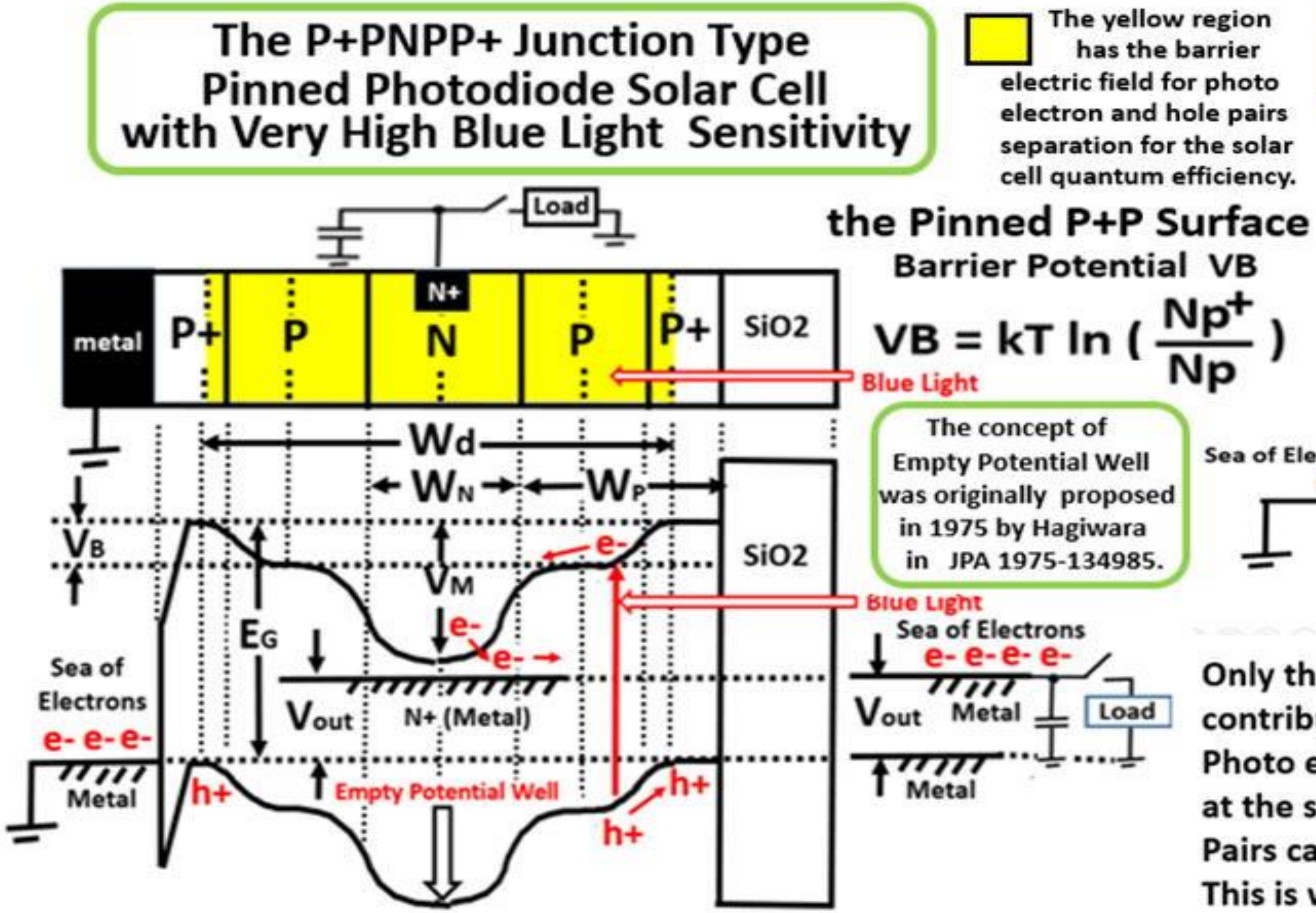
$$HH(x) = N_{PP} \exp\left( - \frac{ZZ(x)}{kT} \right)$$

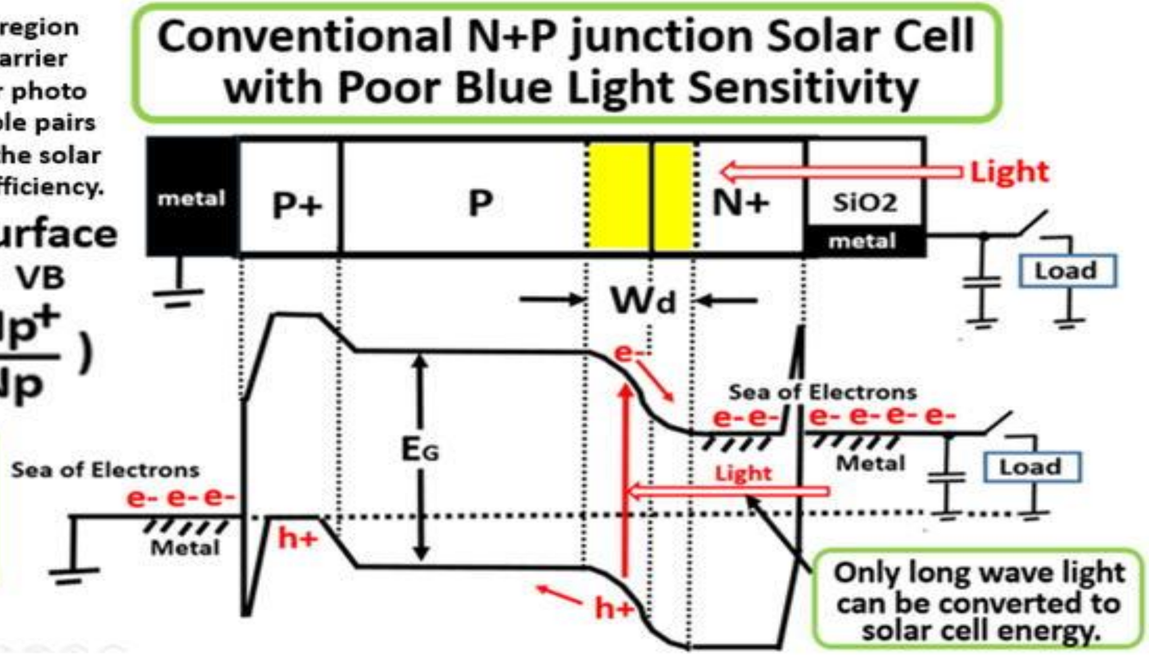
# 8 Double Junction Photo Transistor type Solar Cell

Photo Electron and Hole Pairs Separation at the P+P Pinned Surface Barrier Potential (VB) in a very high quantum efficiency P+PNPP+ junction Pinned Photo Diode Solar Cell proposed and applied for a patent ( JPA 2020-131313 ) by Yoshiaki Hagiwara.



# 8 Double Junction Photo Transistor type Solar Cell




Only the small portion Wd of the N+P junction depletion width can contribute for the quantum efficiency in the conventional solar cell . Photo electron and hole pairs generated by the short wave blue light at the silicon surface are in the sea of electrons of a flat potential level. Pairs cannot be separated without electric field and recombine quickly. This is why the conventional solar cell has a poor quantum Efficiency.

**The surface P+P Pinned Surface Solar Cell with the surface P+P Gaussian doping slope is very important to create the surface barrier electric field for separating the photo electron and hole pairs generated by the short wave length blue light which cannot penetrate into the silicon crystal more than 0.2 μm in depth.**